PDN_Design_Guide

Issued by	Rock-chip	Document Type	Design Guide
Purpose	This document is a guideline for PDN design		
Revision History Date	Version		
10 July 29, 2016	V0.2		

1.Overview

PDN performances were not considered as major criteria in the early of the PCB designs. In today's platform with lower voltage, higher current, smaller voltage noise margin, PDN performances should be estimated early in the PCB design and optimized to meet the device specification.

1.1 PDN theory (1 of 3)

A properly designed PDN helps ensure supply voltage compliance to the required operating conditions of processors and other integrated circuitry.

Proper PDN design ensures that Vmin ≤ V(t) ≤ Vmax during all di/dt events.

• V(t) is the voltage measured at the processor power pins as a function of time.

• Vmin is the minimum voltage allowed (DC + transient) at the processor power supply pins to guarantee proper operation over all variations of process and temperature as listed in the device specification.

• Vmax is the maximum voltage allowed (DC + transient) at the processor power supply pins to guarantee proper operation over all variations of process and temperature as listed in the device specification.

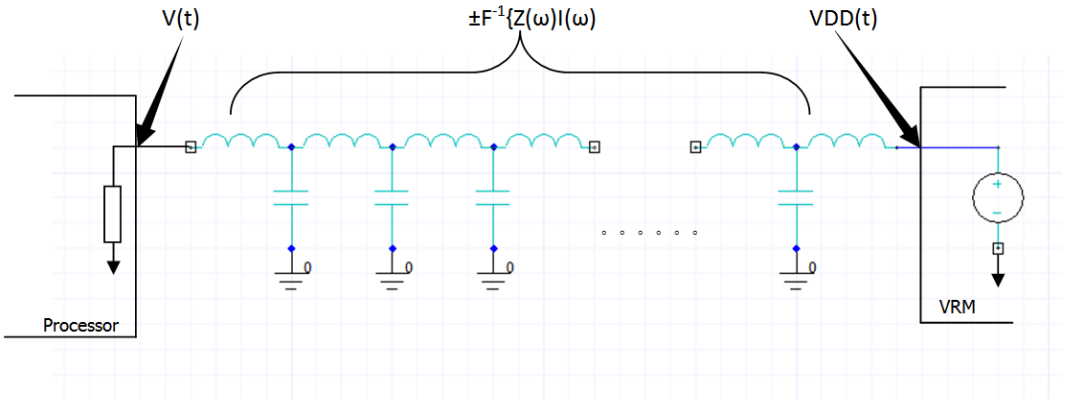

Figure 1

Key formula: $V(t) = VDD(t) \pm F^{-1}\{Z(\omega)I(\omega)\}$, as to figure 1.

VDD (t) is the instantaneous voltage at the VRM output.

I(w) is the load current as a function of frequency.

Z(w) is the impedance of the PDN determined from the load (processor power supply pins), back toward the VRM .

1.2 PDN Theory (2 of 3)

A simple representation of a system power delivery network is shown in Figure 2.

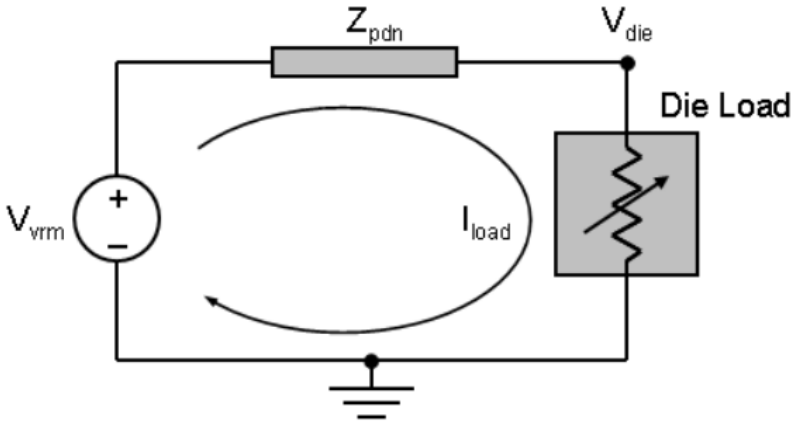

Figure 2. System Power Delivery Network

A power delivery network has an impedance (Z_{PDN}) associated with the path from a voltage regulator module (VRM) to the Processor. The magnitude of noise (voltage ripple) seen on a given power rail is proportional to the impedance (Z_{PDN}) and the transient current ($I_{TRANSIENT}$) draw associated with that rail. Figure 3 shows the schematic representation of $I_{TRANSIENT}$.

Based on Ohms law:

$V_{RIPPLE} = I_{TRANSIENT} * Z_{PDN}$

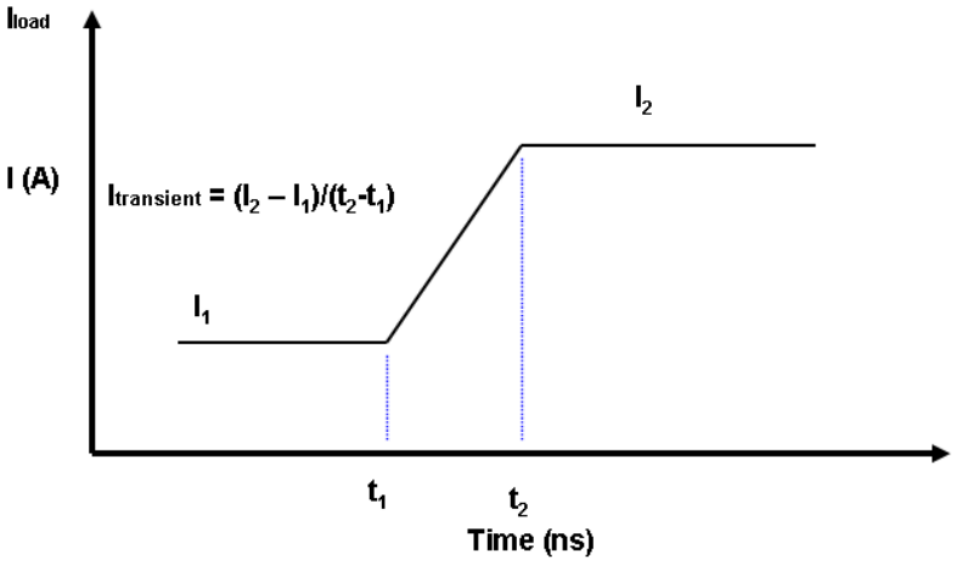

Figure 3. $I_{transient}$ Definition

The transient current is application-specific and is determined by the switching signal pattern. As a board designer, you have no control over this parameter. You can reduce the voltage ripple by reducing Z_{PDN}. The PCB portion of Z_{PDN} is under your control. You can optimize this parameter through good board design practices. To ensure that the voltage ripple noise is within the chip specification, the Z_{PDN} must be designed to meet a certain

impedance, called Z_{TARGET}. Z_{TARGET} acts as your guideline on the magnitude of PCB impedance (Z_{PCB})You can define Z_{TARGET} as follows:

Equation1.

$$Z_{TARGET} = \left[\frac{VoltageRail \bullet \left(\frac{\%Ripple}{100} \right)}{MaxTransientCurrent} \right]$$

Note:

This guide provides a suggested frequency for PCB decoupling. This frequency is called $F_{EFFECTIVE}$. Designing the PCB decoupling beyond this frequency does not result in a system PDN profile improvement. This frequency is calculate by taking into account the PCB, package, and die parasitics.

1.3 PDN Theory (3 of 3)

Figure 4 shows the simple schematic representation of PDN topology .The PCB PDN network contains the following :

(1) Voltage regulator module (VRM)

(2) Decoupling capacitors

(3) Parasitics from power/ground plane spreading, and BGA vias

(4) Plane capacitance

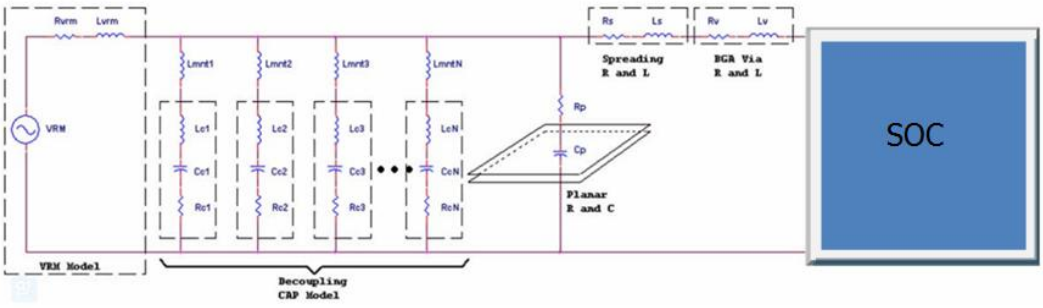

Figure 4. Schematic Representation of PDN Topology

2. Static IR Drop PDN Guidelines

IR drops can happen at every level in a chip, package, and board system. Components that are distant from their associated power source are particularly susceptible to IR drop. It is advised to minimize voltage drop to avoid unacceptable power loss. Early dc assessments help determine power distribution basics such as the best available entry point for power, layer stack up choices, and estimates for the amount of copper needed to carry the current.

DC resistance is determined by the geometry of the net, its material conductivity, refer to Figure 5.

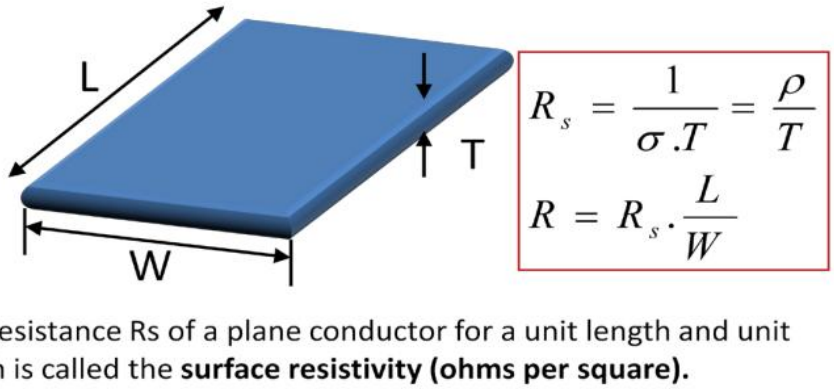

Figure 5: DC resistance

Once DC resistance is determined, IR drop can be calculated with Ohm's law.

$$DC\ IR\ drop = R_{dc} . I$$

An IR drop of 0.5%-2.5% of the nominal voltage is tolerated depending on the total system-level margin allowed for proper device functionality and sense line position.

When power net change layer, it must have enough via to decrease the impedance of power rail ,and develop the current flow capacity. IF via diameter is 0.2mm,it approximately can flow 420mA current .IF power rail transmit 4.2A,we need at least 10 vias when power net change layer.

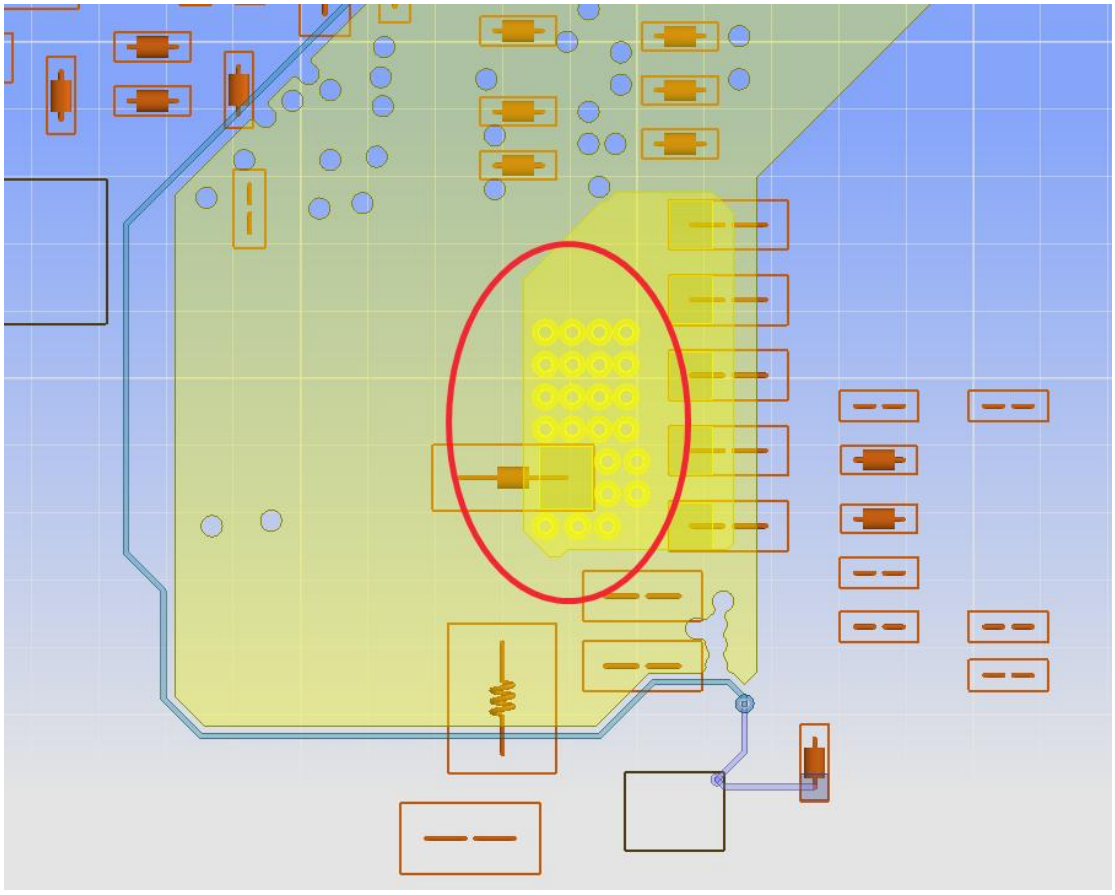

Figure 6: Power rail change layer

Due to the shape geometry complexity, vias and multilayer's used during the net routing, it is difficult to calculate manually the DC resistance. Numerous Signal Integrity (SI) or Layout EDA tools extract the DC resistance.

General recommendations for minimizing DC resistivity:

- Shorten the length of the power nets trace by optimizing VRM and AP (Application Processor) placement but also their balls positioning.

- Avoid discontinuity in power nets trace by inserting other signal nets or matrix of vias with their associated anti-pads within the power nets.

- Avoid via starvation by determining maximum current carrying capacity and numbers of transitional via.

- External trace routing between components must be as wide as possible. The wider the traces the lower the dc resistance and consequently the lower the static IR drop.

3. PCB Stack-up Guidelines

The placement of power and ground planes in the PCB stack up (determined by layer assignment) has a significant impact on the loop inductances of power current path .For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle.

An optimized PCB stack-up for higher power integrity performance can be achieved by following these requirements:

• Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and the ground planes must be solid to provide continuous return path for return current.

• Use a thin dielectric thickness between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) will maximize the capacitance.

• For single-sided PCB ,components is on the top or bottom layer. As Figure 7,components is on top layer.Keep the power and ground plane pair as close as possible to the top layer which components is on . This will help in minimizing the loop inductance. For double-sided PCB ,properly placed and routed back-side capacitors are an effective design option because they can greatly reduce the PDN impedance at high frequencies (> ~10 MHz) when placed as close as possible to the processor power pins. This minimizes the effective inductance associated with those capacitors. It is usually more difficult to place top-side capacitors (on the same side as the processor) with as low an effective loop inductance.

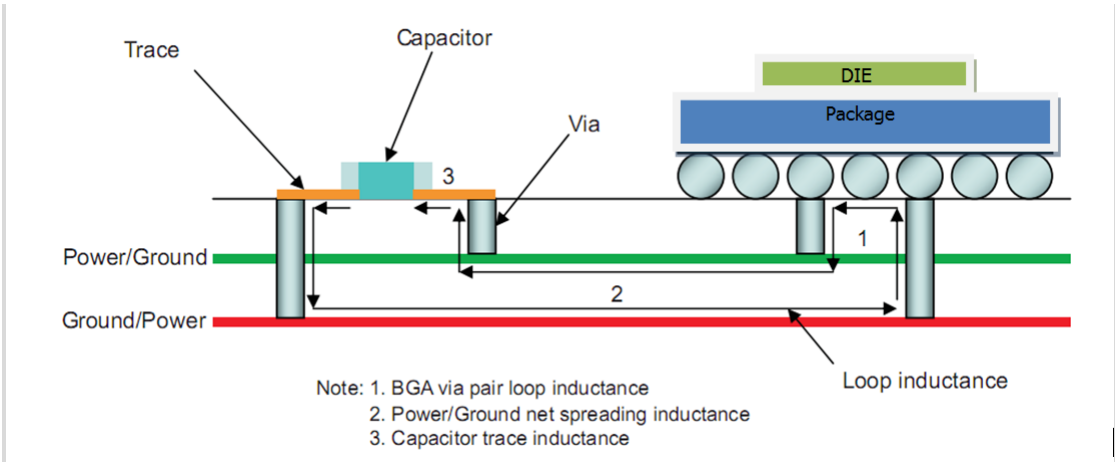

Figure 7. Minimize Loop Inductance With Proper Layer Assignment

As figure 8 , Processor is on the layer1, Better design is which dielectric is thinner and close to layer1 .

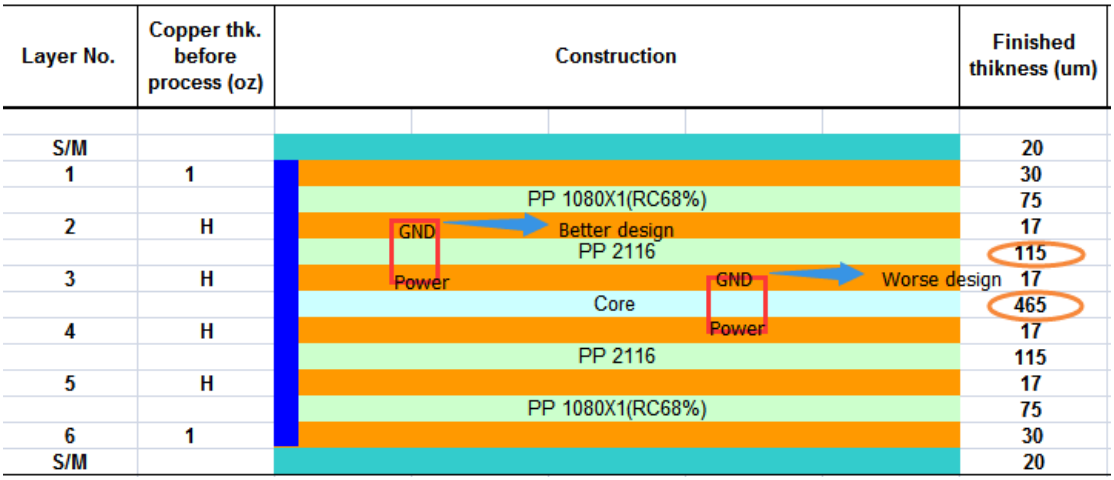

Figure 8

For six layer layout, When Processor is on top layer, we recommend the PCB stack up below .It is advised to put the sensitive and high priority power supplies for example GPU ,BIG_CPU,LIT_CPU ,Center, DDR on the power layer.

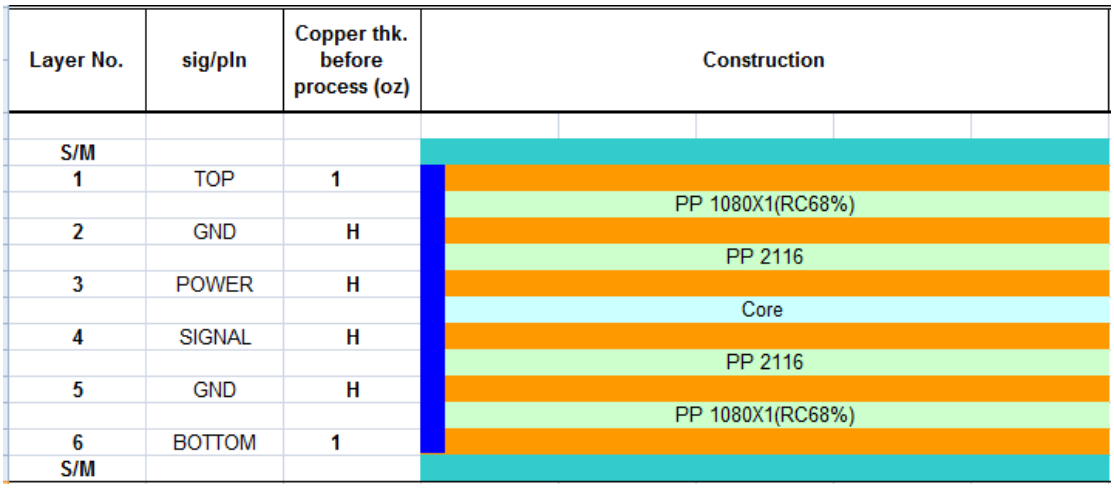

Figure 9. six layer stack up example

For eight layer layout, When Processor is on top layer, we recommend the PCB stack up below .It is advised to put the sensitive and high priority power supplies for example GPU ,BIG_CPU,LIT_CPU, Center, DDR on the power layer.

Layer No.	sig/pln	Copper thk. before process (oz)	Construction
S/M			
1	TOP	1	
			PP 1080X1(RC68%)
2	GND	H	
			Core
3	POWER	H	
			PP 1080X1(RC68%)
4	SIGNAL	H	
			Core
5	GND	H	
			PP 1080X1(RC68%)
6	SIGNAL	H	
			Core
7	GND	H	
			PP 1080X1(RC68%)
8	BOTTOM	1	
S/M			

Figure 10. eight layer stack up example

4. Physical layout guidelines of the PDN

4.1 Decoupling Capacitors

You can model a decoupling capacitor as a series combination of R, L, and C.

（1） R represents the equivalent series resistance (ESR) of the capacitor

（2）L represents the equivalent series inductance (ESL)

（3）C represents the capacitance of the capacitor

Figure 11 shows the frequency response of a capacitor. The equivalent circuit of a capacitor is an RLC series resonant circuit. The self-resonant frequency (SRF) is determined by the L and C of the circuit. This frequency is set by the materials and the construction of the capacitor, as shown in Equation2.

Equation2.

$$F = 1/2\pi\sqrt{LC}$$

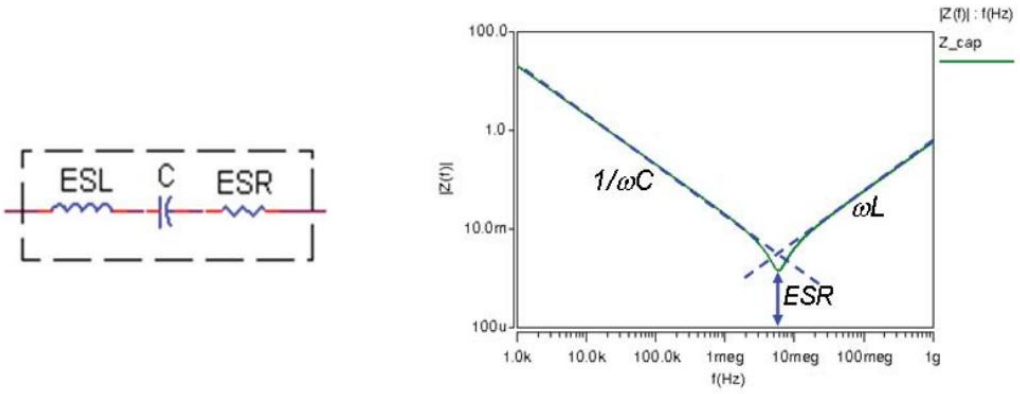

Figure 11. Capacitor Schematic and Frequency Response

Lower power-ground loop area reduces loop inductance thereby improving the effectiveness of a capacitor at high frequencies.

Local decoupling capacitors must be placed as close to the processor pins as possible. As figure 12, double-sided PCB , back-side capacitor has the least loop inductance.

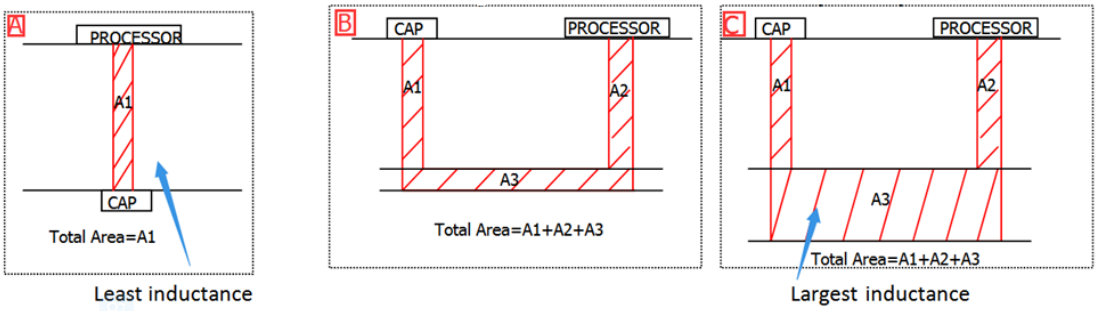

Figure 12

Capacitor effective loop inductance is geometry based.

•Body size influences self-inductance; capacitors with smaller body sizes have lower ESL.

•Locate power-ground vias as close to each other as possible; small loops have lower inductance. As to figure 13.

•Locate vias close to the capacitor terminals; small loops have lower inductance. As to figure 13.

•Multiple parallel power-ground via pair connections reduce mounting inductance; parallel loops have lower inductance.

•Avoid sharing vias with adjacent capacitors; parallel loops have lower inductance, series loops have higher inductance.

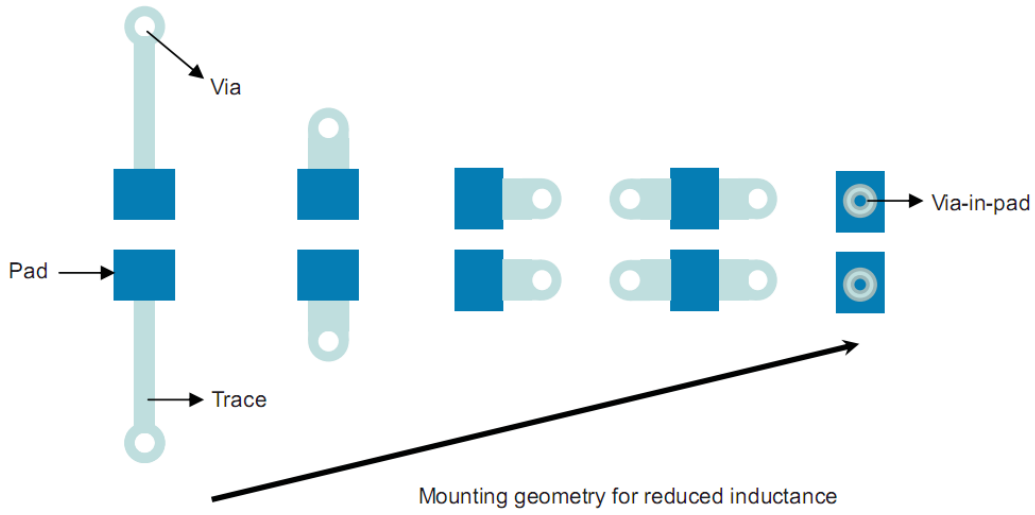

Figure 13

4.2 Parasitics from Power Ground Plane Spreading and BGA Vias

Figure 14 shows the schematic and equivalent representation of spreading and ball grid array (BGA) via inductance. In addition to mounting inductance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance that the capacitor sees with respect to the load. The spreading inductance is design dependent and scales as a function of the dielectric thickness (h) between the power/ground plane. It is determined by the spatial location (d) of the capacitor with respect to the load. Minimizing the dielectric thickness (h) reduces the capacitor location sensitivity and allows you to place the capacitors farther away from the load.

In addition to the spreading inductance from the power/ground planes, current must travel though the via field underneath the BGA before it reaches the Processor. The inductance associated with BGA via is modeled as BGA via inductance. The total inductance seen by any decoupling capacitor is a series combination of the mounting inductance, spreading inductance, and the BGA via inductance.

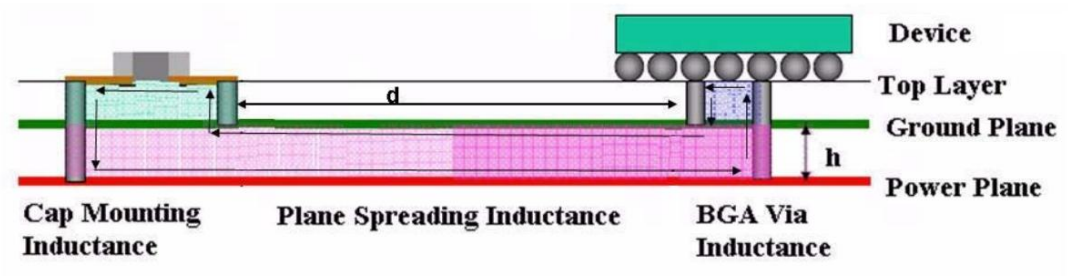

Figure 14. Capacitor Mounting, Spreading Inductance, BGA Via Inductance Schematic

4.2.1 Optimize Loop inductance

The PDN impedance (Z) is modeled by combinations of capacitance, inductance, and resistance. As to figure 15.

Inductor: $Z = j\omega L$

Capacitor: $Z = 1/(j\omega C)$

Resistor: $Z = R$

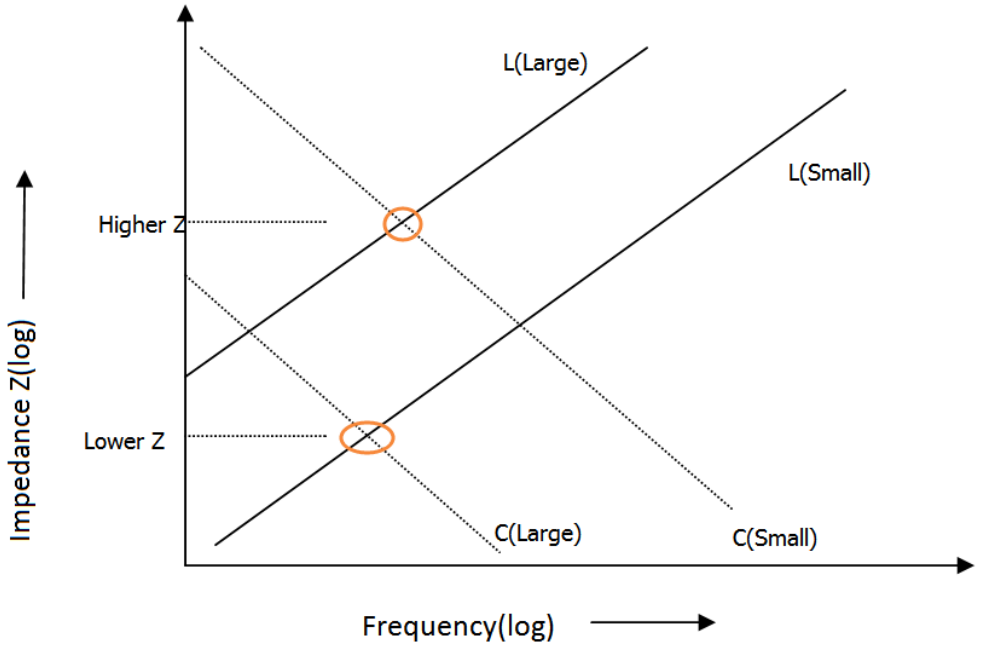

Figure 15

Combinations of larger inductance and smaller capacitance result in a higher impedance. Combinations of smaller inductance and larger capacitance result in a lower impedance.

The amount of loop inductance associated with the PDN routing on a PCB is primarily determined by:

（1）The physical dimensions of the current carrying conductors (power net) and the closeness of the return path (ground net).

（2）The physical dimensions and placement of the passive components connected to the PDN (primarily decoupling capacitors and possibly resistors).

Loop inductance is directly proportional to the area encompassed by a power net and its return path. A large area implies a large loop inductance.Therefore, key steps to reducing loop inductance are:

- Reducing the lengths (x) of both power and ground nets.
- Reducing the vertical distance (y) between power and ground (return) nets.
- Routing multiple current loops in parallel. Ltotal = L1 × L2/(L1 + L2). This is because the parallel loops can support more current for the same voltage drop.
- Wider power and ground (return) traces with broadside (over-under) coupling effectively provide more loops in parallel to reduce inductance.
- Optimally placing and connecting decoupling capacitors. This reduces effective loop area because the capacitors electrically close the parallel inductive branch loops; good placement + connection = smaller loops in parallel.

4.2.2 effect decoupling radius

Small value capacitor must place near Chip pads .Bigger value capacitor can place farther then small value one. Because different value capacitor has different effective decoupling space. If capacitor place far from Chip pads, the distance may beyond the capacitor effective decoupling radius .The capacitor will lose decoupling capacity. The best way to understand decoupling radius is to see the phase between the sudden spike in the current demand and capacitor compensation current. It take time for capacitor to know current demand happen .And transmit compensation current to the current demand place also take time. Because it need time for current transmit in medium .So it absolutely make phase different from the demand current and compensation current. It is best for capacitor to compensation to the demand current of which frequency is same to the capacitor self-resonant frequency f_0 after place on PCB. The f_0 is determined by capacitor loop inductance and the value of capacitor. The wave length of f_0 is λ .According to experiences, the distance from the place of current demand to the place of capacitor had better control in $\lambda/40$ ~$\lambda/50$.

For example placing a 1nF capacitor on the PCB, The loop inductance (which include equivalent series inductance of capacitor itself, mounting inductance, spreading inductance, and the BGA via inductance)is 1.6nH. The self-resonant frequency after placing on the PCB is 125.8MHz, Suppose that the speed of PCB is 166ps/inch, so wave length λ is 47.9 inches. The capacitor effect decoupling radius is $\lambda/50$=0.958 inch. If the distance from 1nf capacitor to the demand current place of chip is beyond 0.958 inch, then the capacitor decoupling capacity is weaken.

4.3 Plane Capacitance

The amount of distributed capacitance seen by the power/ground sandwich is dependent on the following factors:

（1） Length of the plane

（2）Width of the plane

（3）Dielectric constant

（4）Dielectric thickness

You can approximate the amount of capacitance by using a parallel plate capacitor equation, as shown in Equation3. Figure 16 shows the equivalent representation of the plane capacitance between the power/ground sandwich.

Equation3.

$$C = \frac{\varepsilon_0 * \varepsilon_r * W * l}{h}$$

Where ε_0 = permittivity of free space = 0.225pf/inch

ε_r = relative permittivity (dielectric constant) of the dielectric material

W = width of the power plane in inches

l = length of the power plane in inches

h = distance between the power/ground plane in inches

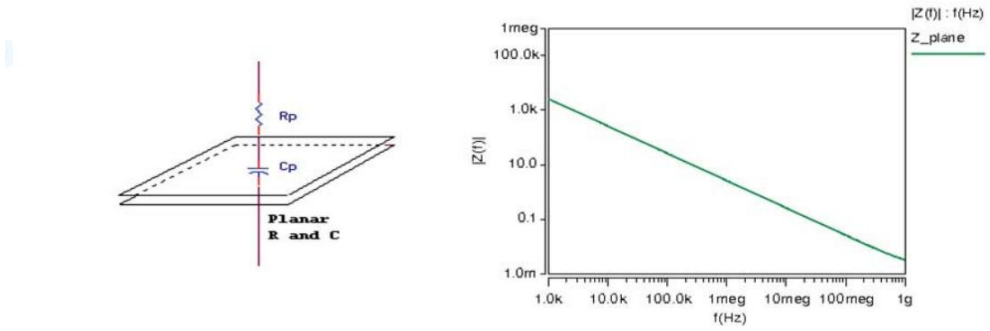

Figure 16. Plane Capacitance Schematic and Frequency Response

For single side PCB ,Plane Capacitance is very useful, It can effectively reduce the high frequency PDN impedance , As figure 17.

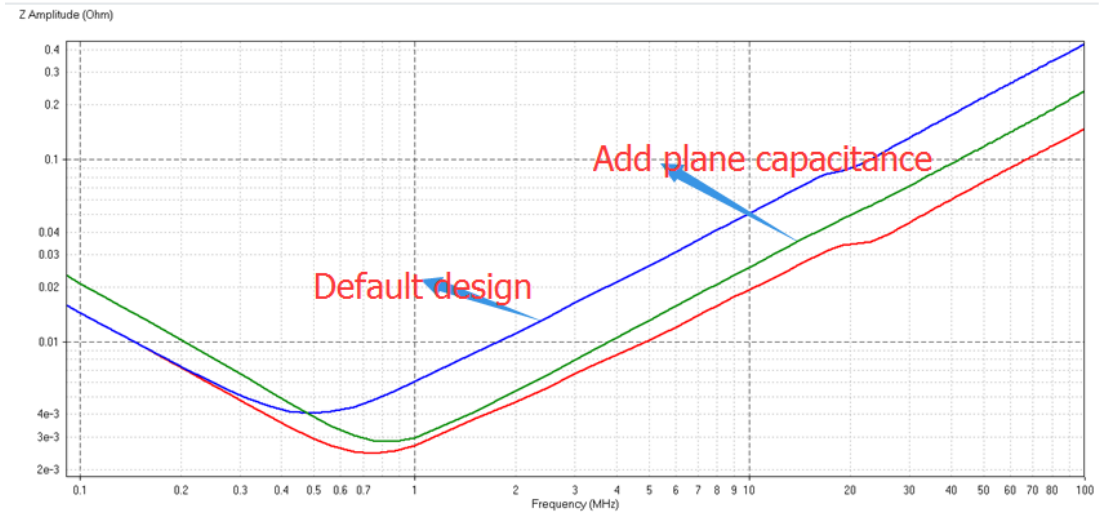

Figure 17

5.General recommendations for PCB Design

A critical step in designing an optimized PDN is that proper care must be taken to ensure that the initial layout is planned with good power integrity design guidelines in mind. The following points are important requirements that will be needed to be implemented in the PCB PDN design:

• When a capacitor is mounted on a PCB, there is additional loop inductance associated with the capacitor mounting. The value of this loop inductance is design-dependent. Figure 18 shows the capacitor placement geometry for improved mounting inductance.

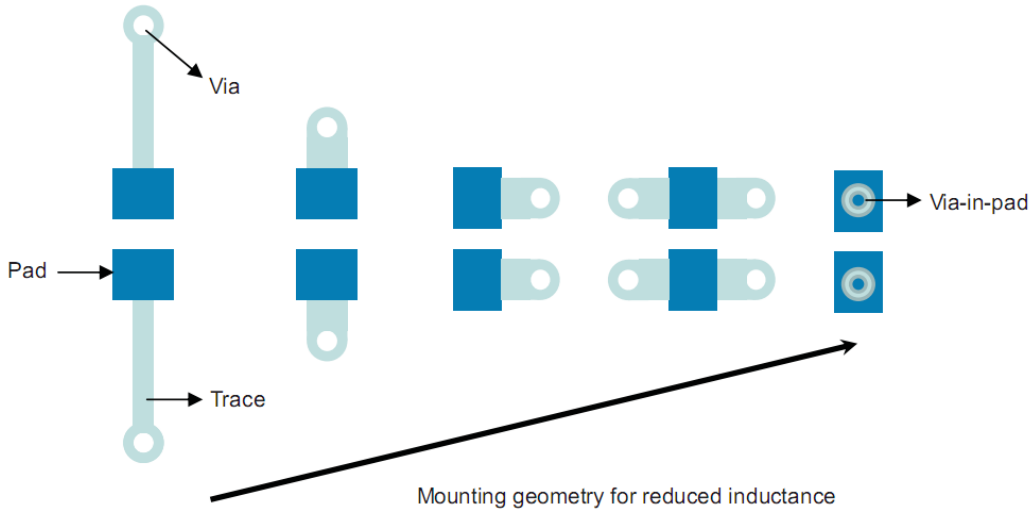

Figure 18. Capacitor Placement Geometry for Improved Mounting Inductance

• As to figure 18,place the vias as close as possible to the capacitor. Minimize the via pitch between the power and ground vias. If possible, use multiple power/ground via pairs. If the PCB manufacturing processes allow and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

For Capacitor parallel loops have lower inductance, series loops have higher inductance.

• Placing power and ground plane pairs closer to the surface where the capacitor is mounted. This minimizes the via length. So minimizing the capacitor loop inductance

• Select capacitors with small footprint to minimize ESL. It helps to minimizing the capacitor loop inductance

• When selecting the capacitors, choose capacitors with multiple values rather than a large number of capacitors of the same value to meet your target impedance. The impedance peaks in Z-profile are formed by resonance behavior within the power delivery network. High ESR at resonance frequency helps in damping the resonance, thereby reducing the magnitude of the impedance peak. Using a large number of capacitors of the same value significantly reduces the ESR near a capacitor SRF and results in a higher magnitude of nearby impedance peaks. Choosing capacitors with multiple values helps maintain a relative

high ESR over a wide frequency range. As to figure 19,we can see multiple values capacitors ,the PDN curve is more smooth then using a large number of capacitors of the same value .

One per decade		Three per decade	
10 μF	2	10 μF	1
		4.7 μF	2
		2.2 μF	1
1 μF	3	1 μF	1
		0.47 μF	1
		0.22 μF	1
0.1 μF	4	0.1 μF	2

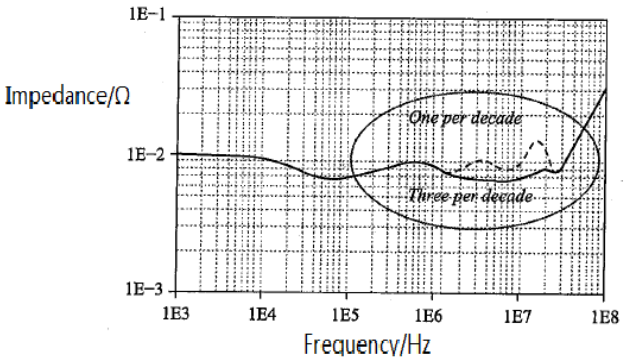

Figure 19

• Use short, wide surface traces to connect the capacitor or Chip pads to the vias. Place vias as close to Chip pads.

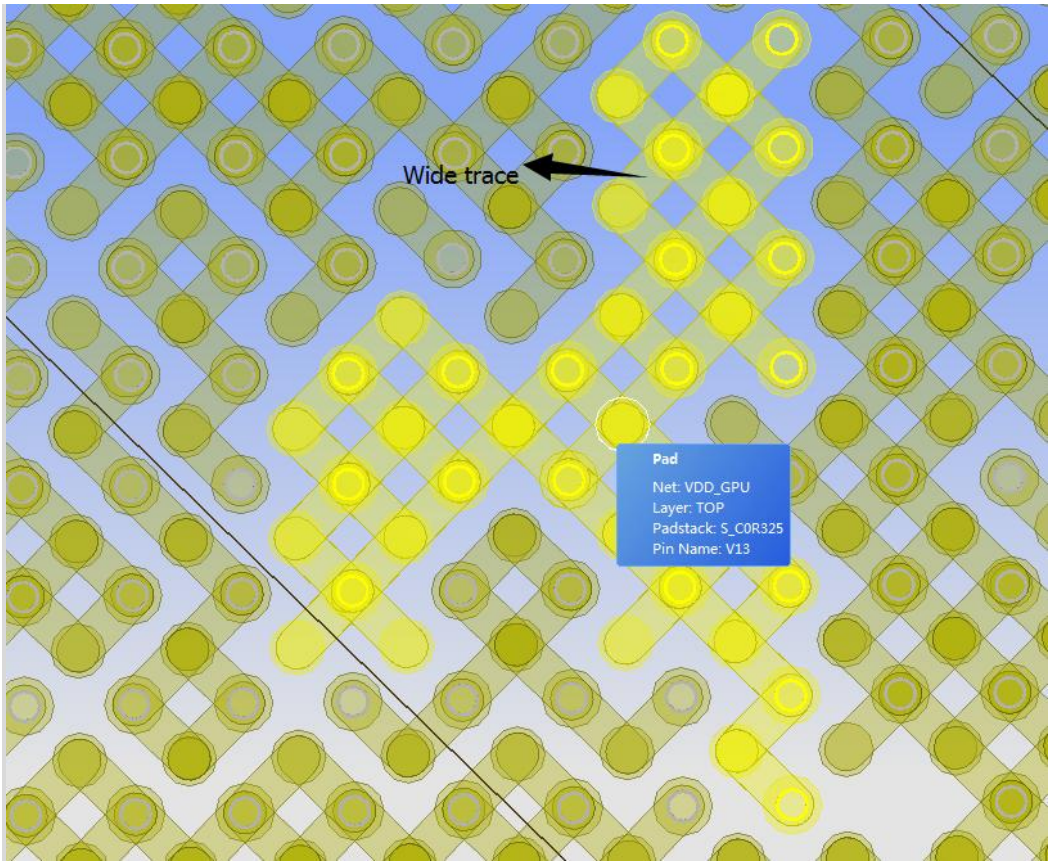

Figure 20 .wide surface trace connect Chip pads to the vias

Minimize the dielectric thickness between the power/ground plane. When designing the board stack up, ensure that the power/ground layers are next to one another. Keep the

power and ground plane pair as close as possible to the top and bottom surfaces This will help in minimizing the decoupling capacitors mounting, via, and the power /ground plane pair spreading loop inductance.

• Choose the placement of the high-frequency capacitors so that you minimize the overall loop inductance. This overall inductance is a combination of capacitor ESL, capacitor mounting, capacitor spreading, and BGA via inductance. Give high-priority placement to high-frequency capacitors when compared with mid-and low-frequency capacitors. Place high-frequency decoupling capacitors closed to Chip. The mid- and low-frequency capacitors are less sensitive to placement. They can be placed farther from the Chip when compare with high-frequency capacitors. But it is suggested to place them as close as possible to Chip to minimizing the capacitor loop inductance.

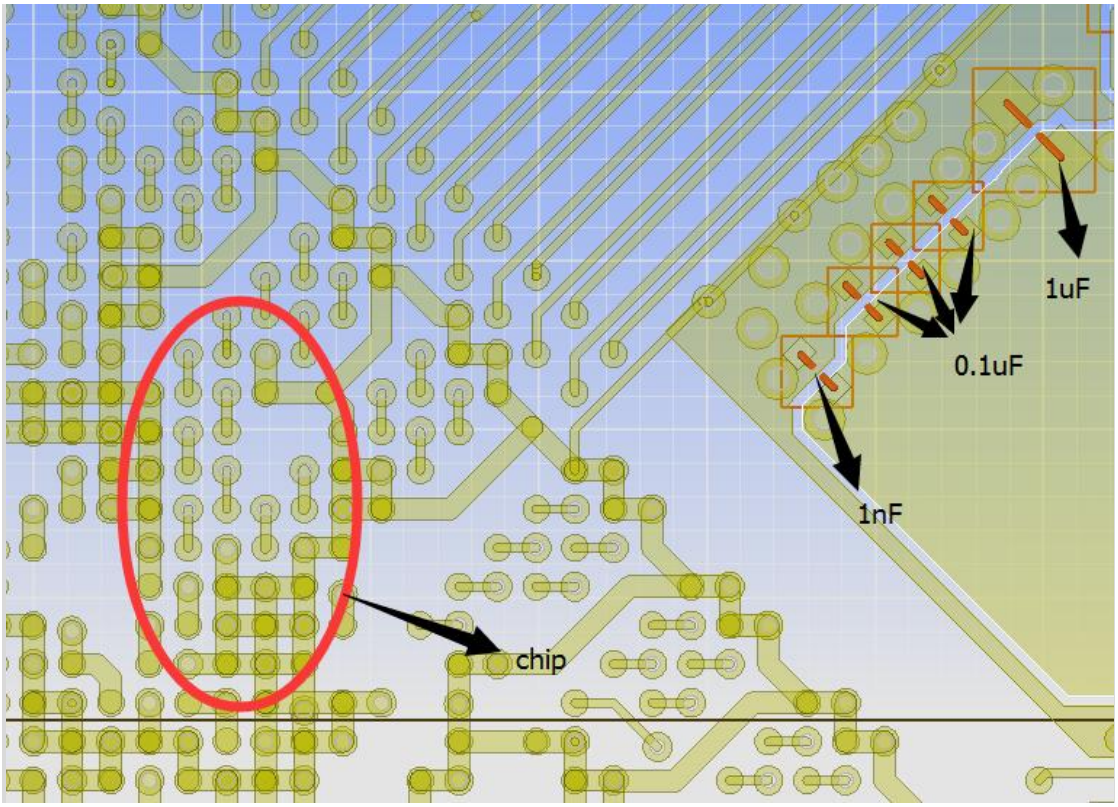

Figure 21 .high-frequency capacitors place closer to RK3399

•When carving plane shapes, ensure the plane shapes are reasonably square in shape. Avoid having a long and narrow plane shape because this limits the current flow and increases plane spreading inductance.

• Whenever possible, try aiming for a ratio of 1:1 or better for component (for example, capacitors , resistors, Chip pads) pads and vias. And use wide trace to connect same net's pads and vias together. Do not share vias among multiple capacitors. Do not share vias

among multiple pads of Chip.

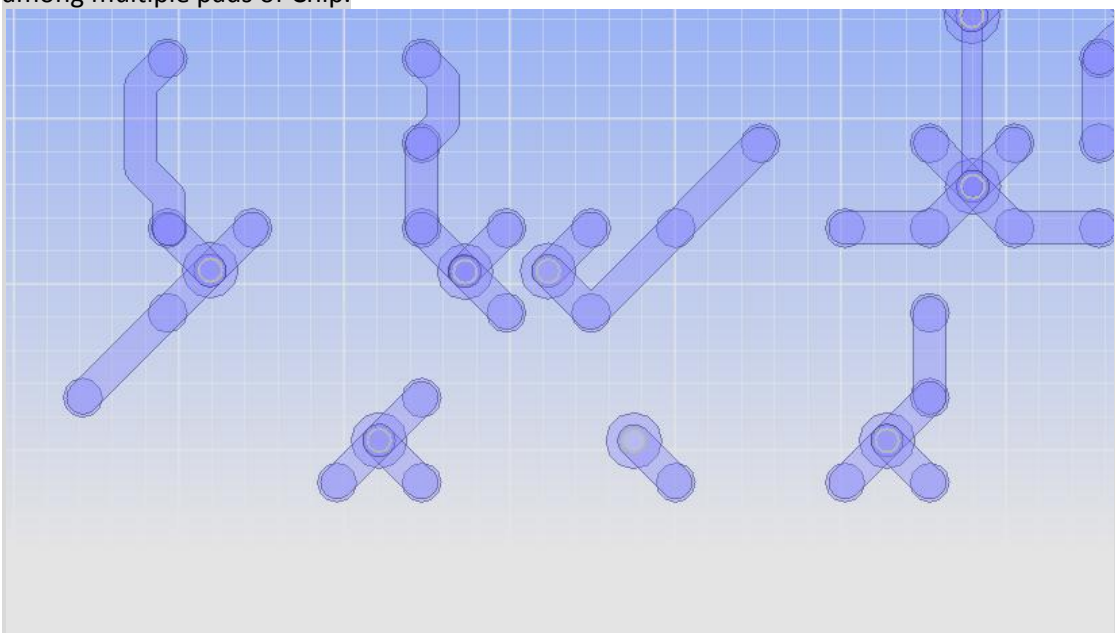

Figure 22. Do not share vias among multiple pads

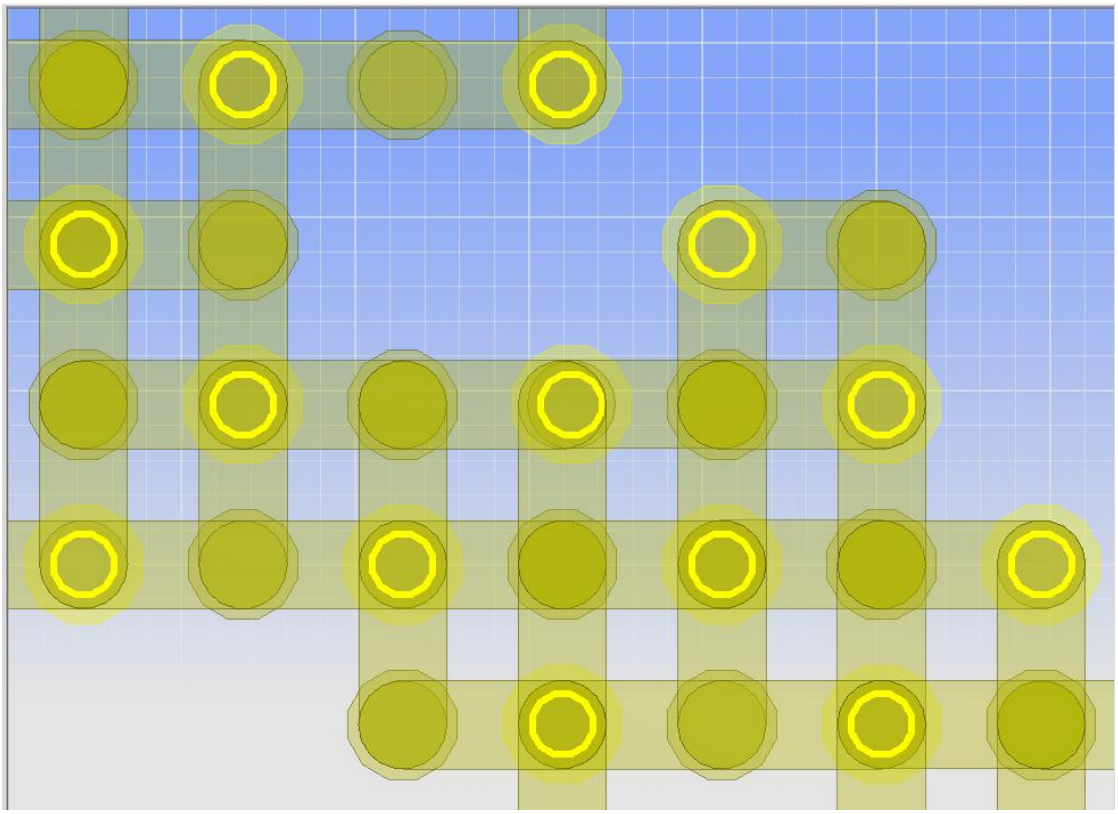

Figure 23. At least one pad one via AND use wide trace connect them together

• To avoid the maximum current carrying capacity of each transitional via, an evaluation must be performed to determine the appropriate number of vias required to connect components. Figure 24 and Figure 25 show examples of via starvation on a power net transitioning from top routing layer to internal layers and the improved layout, respectively.

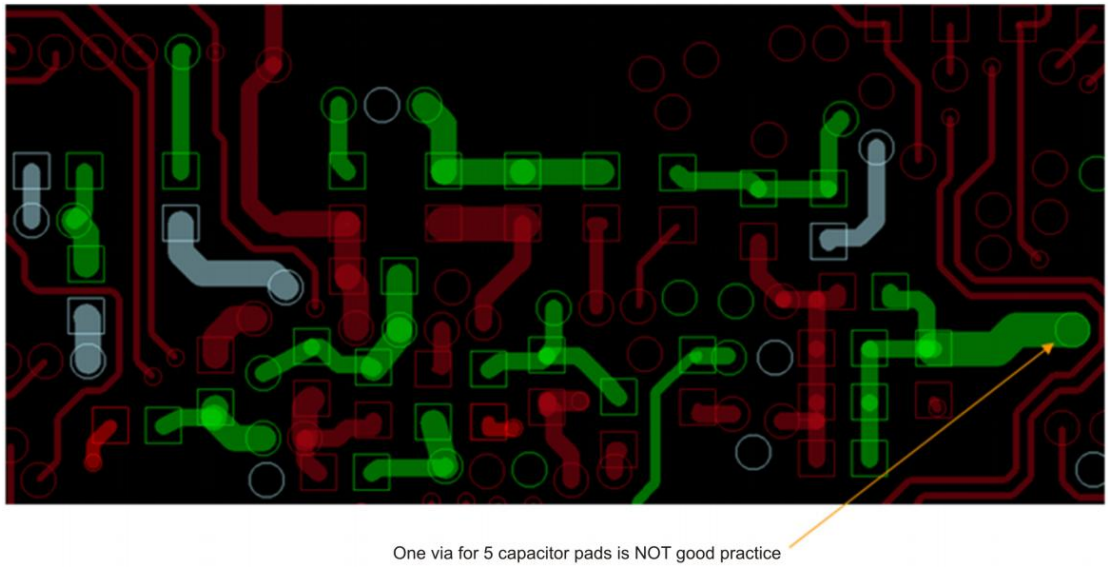

Figure 24. Via Starvation

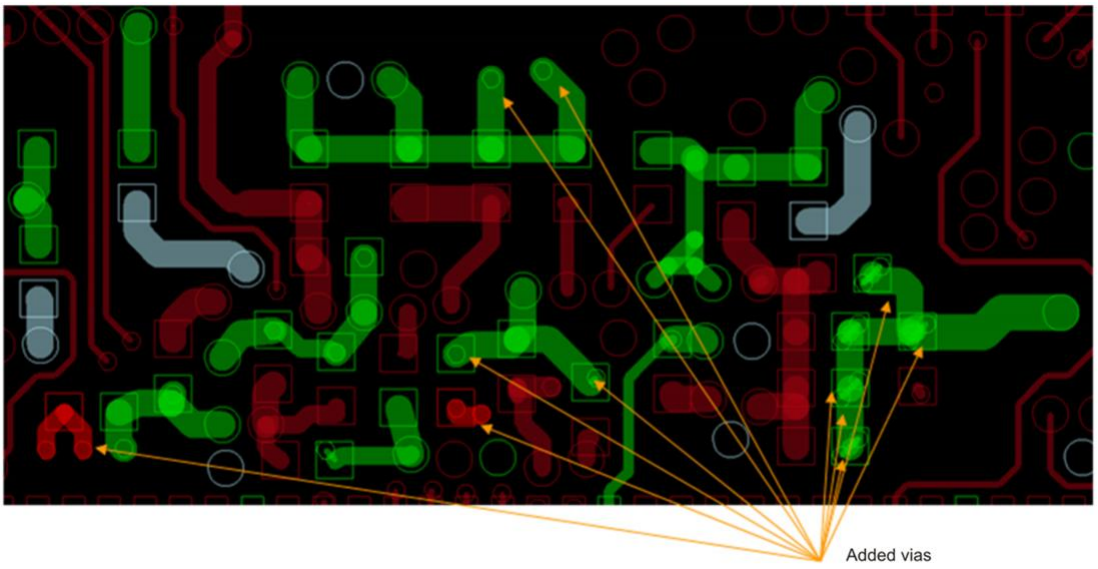

Figure 25. Improved Layout With More Transitional Vias

• It is strongly advised that the current first passes the bypass capacitor and then enters the supply pin.

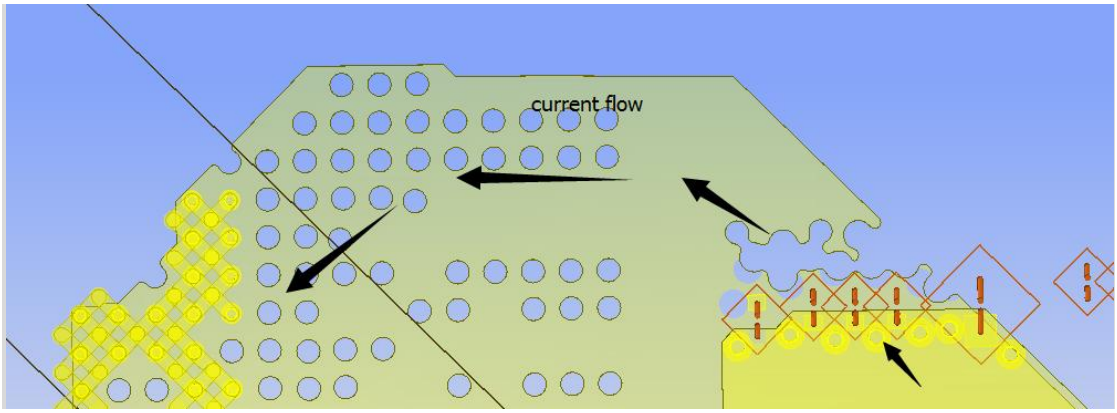

Figure 26. Current first passes the bypass capacitor then enters the supply pin

• Shorten the length of the power nets trace by optimizing VRM and AP (Application Processor) placement but also their balls positioning.

• Avoid discontinuity in power or GND nets trace by inserting other signal nets or matrix of vias with their associated anti-pads within the power or GND nets. It is strongly advised to keep the power plane and return path plane completely to provide continuous return path. The unused pads of vias in inner layers should be removed ,it will help to avoid discontinuity in power or GND plane.

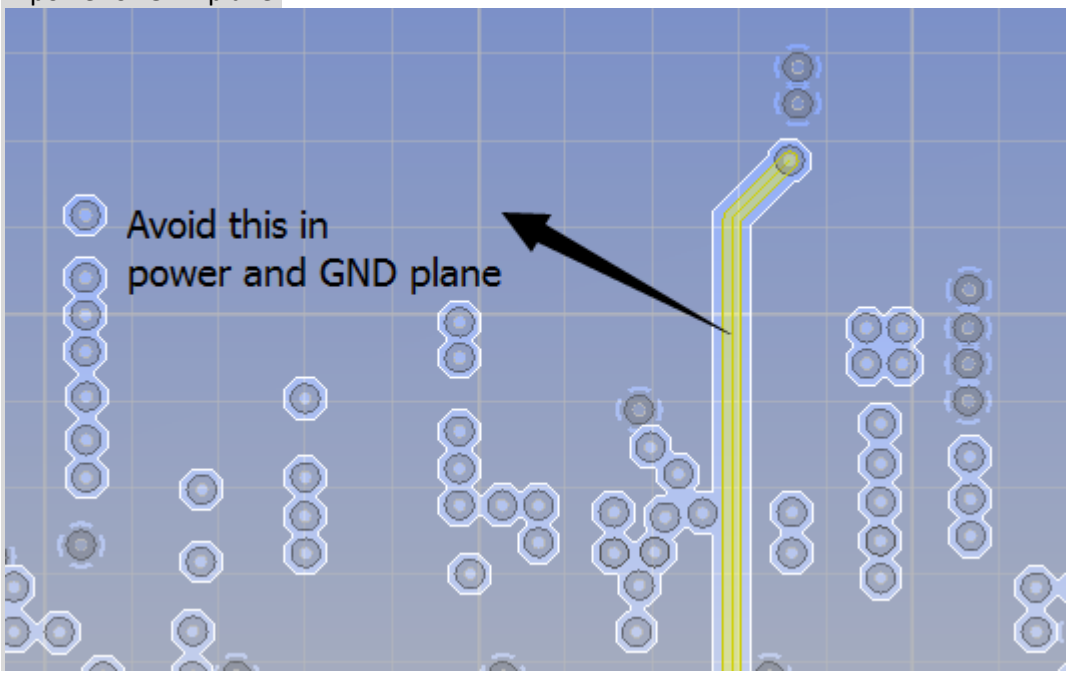

Figure 27. Avoid inserting other signal nets in power or GND plane

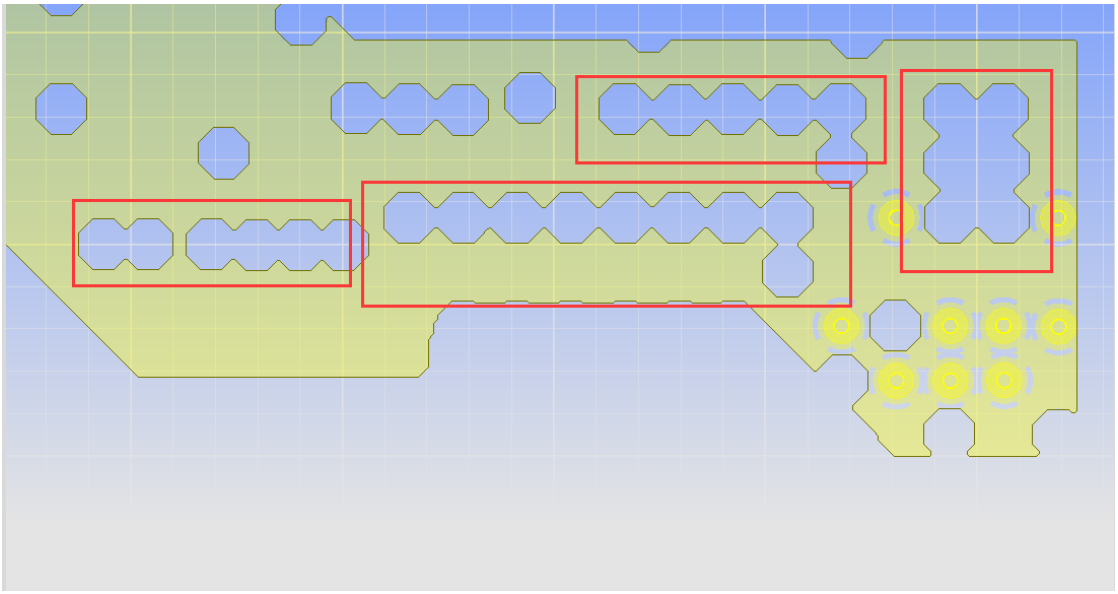

Figure 28. matrix of vias with their associated anti-pads discontinuity plane

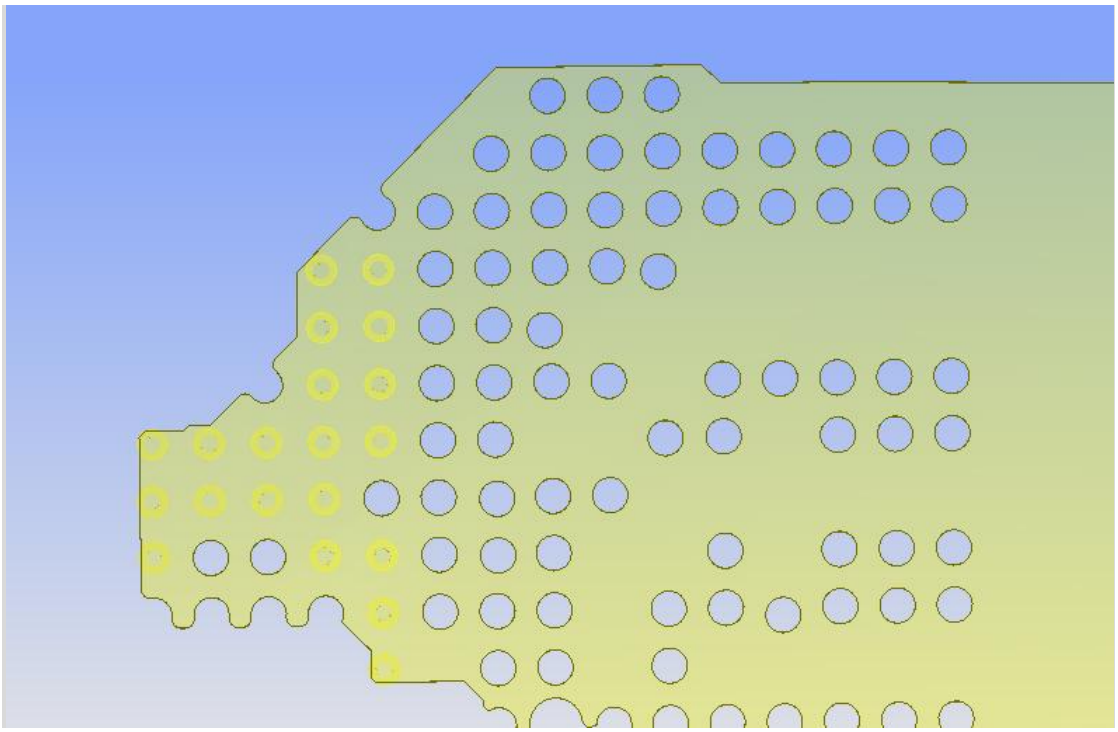

Figure 29 Unused pads of vias in inner layers removed and avoid matrix of vias

Signal vias create voids in the power and ground planes. Improper placement of vias can create plane areas in which the current density is increased. These areas are also called hot spots. It is important to avoid these hot spots. Often a good approach is to place the vias in a grid that leaves enough space between the vias for the power plane to pass

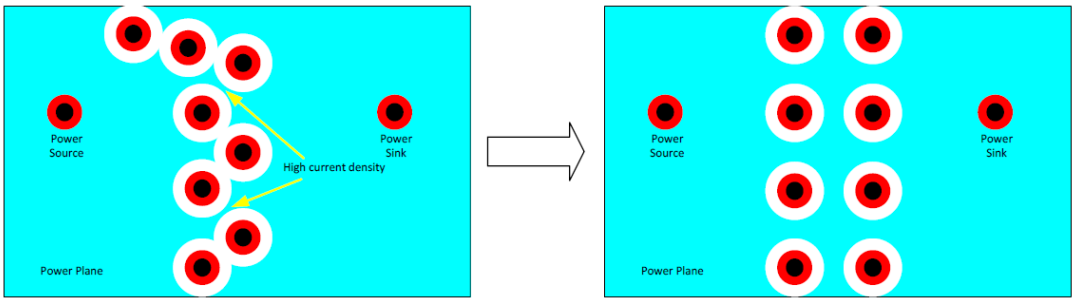

Figure 30: Avoid Copper Plane Hot Spots

• External trace routing between components must be as wide as possible. The wider the traces the lower the dc resistance and consequently the lower the static IR drop.

• The feedback of power rail line, should route on the same layer with power rail. And come out with the power rail plane. Make sure feedback line will nor disturb by other nets .

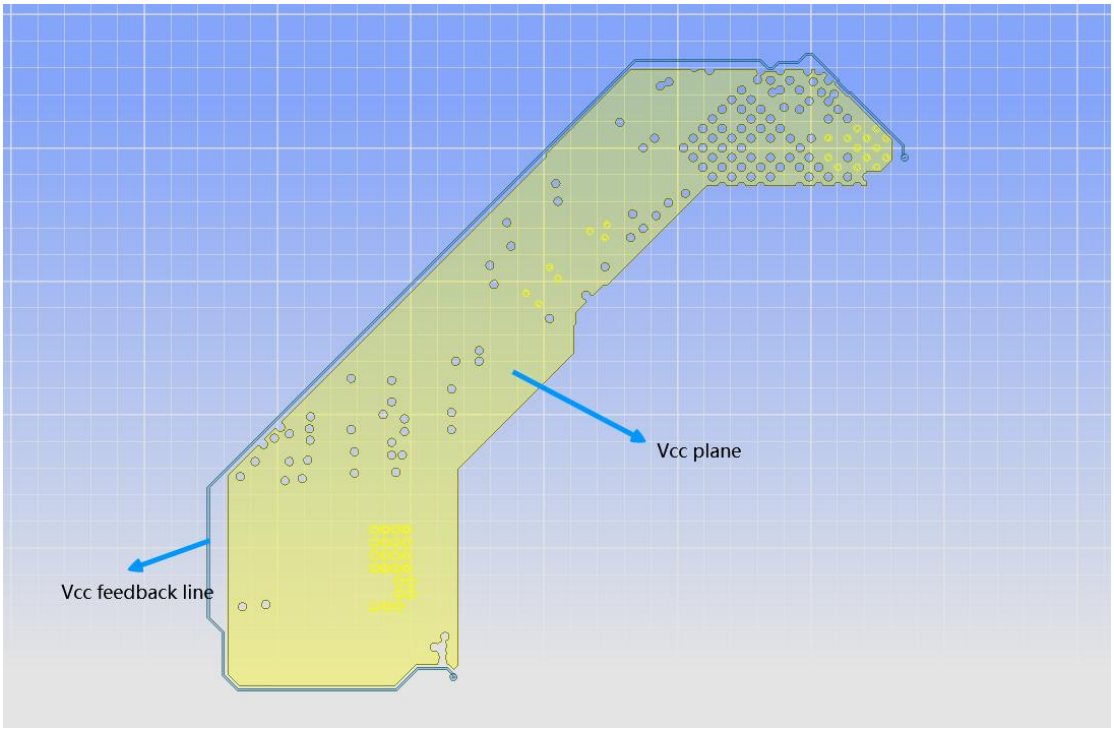

Figure 31. Power feedback line

For double-sided PCB ,properly placed and routed back-side capacitors are an effective design option because they can greatly reduce the PDN impedance at high frequencies (> ~10 MHz) when placed as close as possible to the processor power pins. This minimizes the effective inductance associated with those capacitors. It is usually more difficult to place top-side capacitors (on the same side as the processor) with as low an effective loop inductance.It is effective way to add plane capacitance to reduce the PDN impedance at high frequencies. So make the power and gnd plane as wider as possible.