Layout Design Guide

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Purpose	This document is a guideline for designing a carrier board with high speed signals that is used With Rk3399 chip		
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1 Introduction

1.1 Overview

The RK3399 chip features high speed interfaces such as PCI Express, HDMI, USB 3.0 ,DP,and EDP which require special layout considerations regarding trace impedance and length matching. Improper routing of such signals is a common pitfall in the design. This document helps avoiding layout problems that can cause signal quality or EMC problems. Please read this document very carefully before you start designing a carrier board.

1.2 Abbreviations

Abbreviation	Explanation
EMC	Electromagnetic Compatibility -theory of unintentional generation, propagation, and reception of electromagnetic energy
EMI	Electromagnetic Interference - high frequency disturbances
GND	Ground
HDMI	High-Definition Multimedia Interface - it combines audio and video signal for connecting monitors, TV sets or Projectors, electrical compatible with DVI-D
MIPI	Mobile Industry Processor Interface Alliance
PCIe	PCI Express - high-speed serial computer expansion bus that replaces the PCI bus
USB	Universal Serial Bus - serial interface for internal and external peripherals
VCC	Positive supply voltage
DP	Display port
EDP	Embedded Display Port
USIC	High-speed inter-chip USB

Table 1: Abbreviations

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2 PCB Stack-Up

In order to reduce reflections at high speed signals, it is necessary to match the impedance between source, sink, and transmission line. The impedance of a signal trace depends on its geometry and its position with respect to any reference planes. The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depends on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized. The presented stack-up in the following subsection is intended as example which can be used as a starting point for helping in stackup evaluation and selection. If a different stack-up is required other than those shown in the examples, please recalculate the dimensions of the traces. Work closely with your PCB manufacturer when selecting suitable stack-up solution.

2.1 Eight Layer Stack–Up

Layer No.	sig/pln	Copper thk. before process (oz)	Construction	Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M				20	0.79	+/-10	3
1	TOP	1		30	1.18	+/-10	
			PP 1080X1(RC68%)	75	2.95	+/-10	3.8
2	GND	H		17	0.67	+/-10	
			Core	365	14.37	+/-10	4.2
3	POWER1	H		17	0.67	+/-10	
			PP 2116X1(RC68%)	115	4.53	+/-10	3.8
4	POWER2	H		17	0.67	+/-10	
			Core	265	10.43	+/-10	4.2
5	GND	H		17	0.67	+/-10	
			PP 2116X1(RC68%)	115	4.53	+/-10	3.8
6	SIGNAL	H		17	0.67	+/-10	
			Core	365	14.37	+/-10	4.2
7	GND	H		17	0.67	+/-10	
			PP 1080X1(RC68%)	75	2.95	+/-10	3.8
8	BOTTOM	1		30	1.18	+/-10	
S/M				20	0.79	+/-10	3

Figure 1: Eight Layer PCB Stack-Up Example

The signals on the top layer are referenced to the plane in Layer 2, while the signals on the bottom layer are referenced to layer 7. The ground planes on Layer 5 and 7 are used as references for the high-speed signals routed on Layer 6.

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3 Trace Impedance

Care should be taken to distinguish between single-ended and differential trace impedance. High-speed single ended signals such as the LPDDR3 need to be routed with the specified single-ended impedance. This is the impedance between the trace and the reference ground.

High-speed differential pair signals such as PCIe, EDP,USB, HDMI etc. need to be routed with differential impedance. This is the impedance between the two signal traces of a pair. As the signals are also referenced to ground, each differential pair signal also has single-ended impedance. When selecting trace geometry, priority should be given to matching the differential impedance over the single-ended impedance. The differential impedance is always smaller than twice the single ended impedance.

When defining trace geometry, try to keep the calculated impedance value as close as possible to the exact impedance value. This allows greater flexibility during PCB manufacture. Variation in impedances will occur between different production lots. If the calculated impedance is in the middle of the tolerance band, it will help ensure the maximum production yield.

Traces on the top or bottom layer have only one reference plane. These traces are called Microstrip. The following figure shows the geometry of such Microstrips. H1 is the distance from the trace to the according reference plane. Er1 is the relative permittivity of the isolation material. The traces have a trapezoid form due to the etching process. In the layout tool, the traces have to be designed with a width of W1. W2 depends on the trace height (T1) and the duration of the etching. Contact your PCB manufacturer in order to get the information about the resulting width W2. S1 is the spacing within a differential pair.

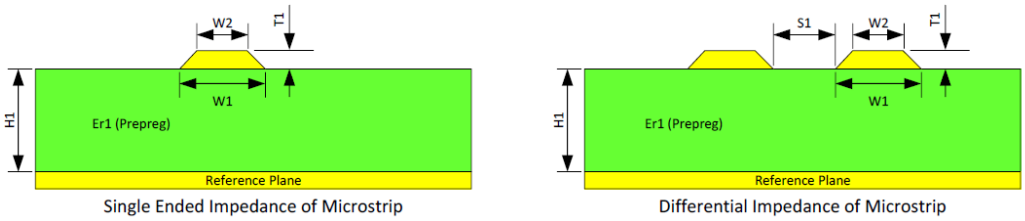

Figure 2: Trace Geometry of Microstrips

Conformal coating is a protective non conductive dielectric layer that is applied onto the printed circuit board . Its purpose is to protect electronic circuits from harsh environments that may contain moisture and or chemical contaminants. The coating material will affect the top and bottom Trace impedance. The following figure shows the geometry of coated Microstrips.C1is the coating height above substrate .C2 is the coating height above trace.C3 is the height of coating between traces. CEr is the coating dielectric.

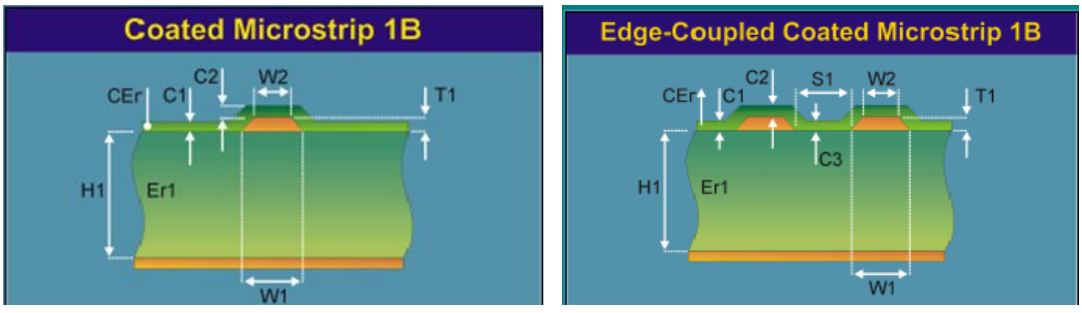

Figure 3: Trace Geometry of coated Microstrips

Traces in the inner layer of a PCB have two reference planes, reducing electromagnetic emissions and increasing immunity to external noise sources. These traces are called striplines. The following figure shows the geometry of such striplines. When making impedance calculation of striplines, special care needs to be taken when it comes to the isolation thickness H1 and H2. H1 is the thickness of the core material. The traces

are embedded in the prepreg material. As the traces have a finite height, the prepreg height H2 depends on the copper density. The relative permittivity of the core and prepreg material can be slightly different. Many impedance calculation tools can take this in account.

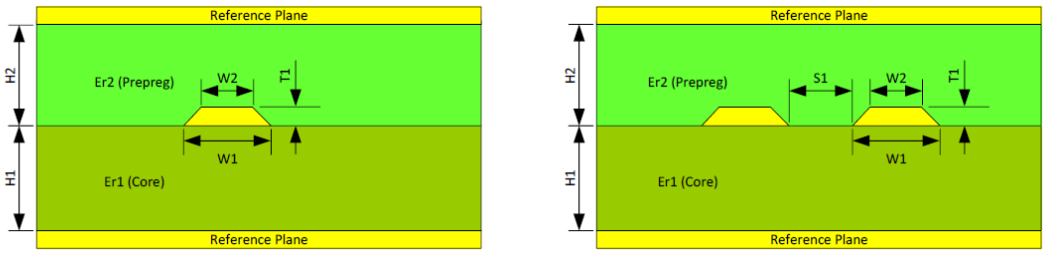

Figure 4: Trace Geometry of Striplines

The following table shows impedance for traces used in the eight layer stack-up, presented in section 2.

layer	Impedance Type	W1(trace width)	S1(spacing within a differential pair)	Required impedance	Imdedance without coated layer	Impendence with coated layer
L1	$Z_{Single\ Ended}$	4mil		50Ω	58.88	55.9
L8	$Z_{Single\ Ended}$	4mil		50Ω	58.88	55.9
L4	$Z_{Single\ Ended}$	4mil		50Ω	56.11	56.11
L6	$Z_{Single\ Ended}$	4mil		51Ω	54.56	54.56
L1	$Z_{differential}$	4mil	4mil	100Ω	101.4	93.73
L8	$Z_{differential}$	4mil	4mil	100Ω	101.4	93.73
L4	$Z_{differential}$	4mil	4mil	100Ω	90.49	90.49
L6	$Z_{differential}$	4mil	4mil	101Ω	91.07	91.07
L1	$Z_{differential}$	5mil	6mil	90Ω	96.75	91.08
L8	$Z_{differential}$	5mil	6mil	90Ω	96.75	91.08
L4	$Z_{differential}$	5mil	6mil	100Ω	88.91	88.91
L6	$Z_{differential}$	5mil	6mil	100Ω	89.93	89.93

Table 2: Eight Layer Stack-Up impedance Example

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4 Component Placement and Schematic Optimizations

The placement of the components is very often an underestimated subtask of the PCB design. Problems with signal return paths are very often related to suboptimal placement of the components. If a signal needs to cross a splitting of its reference plane, one should first check whether this splitting is really unavoidable. Quite often, the solution can be a better placement of the components.

The high-speed signal connection should play a major role in the decisions that are taken during the placement. A minimum amount of vias should be used in high speed interfaces. This means the number of layer changes should be kept as low as possible. When placing the components, try to avoid the need of crossing high-speed signals.

When placing the components, take in account that high-speed signals normally need to have more spacing than other signals. The need of a complicated reference plane shape is often a good indication that the component placement is suboptimal. Do not be afraid of doing placement and routing iterations.

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5 High-Speed Layout Considerations

5.1 crystal Routing

When designing the printed-circuit board: Keep the crystal as close as possible to the crystal pins. Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup. Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
On the top layer place a guard ring around the crystal and tie the ring to on an adjacent ground layer by via to help isolate the crystal from unwanted noise pickup. We also place a guard ring on the package. The second layer is a whole ground layer without any Split Plane .It help to shield crystal from unwanted pickup from traces on other layers of the board.

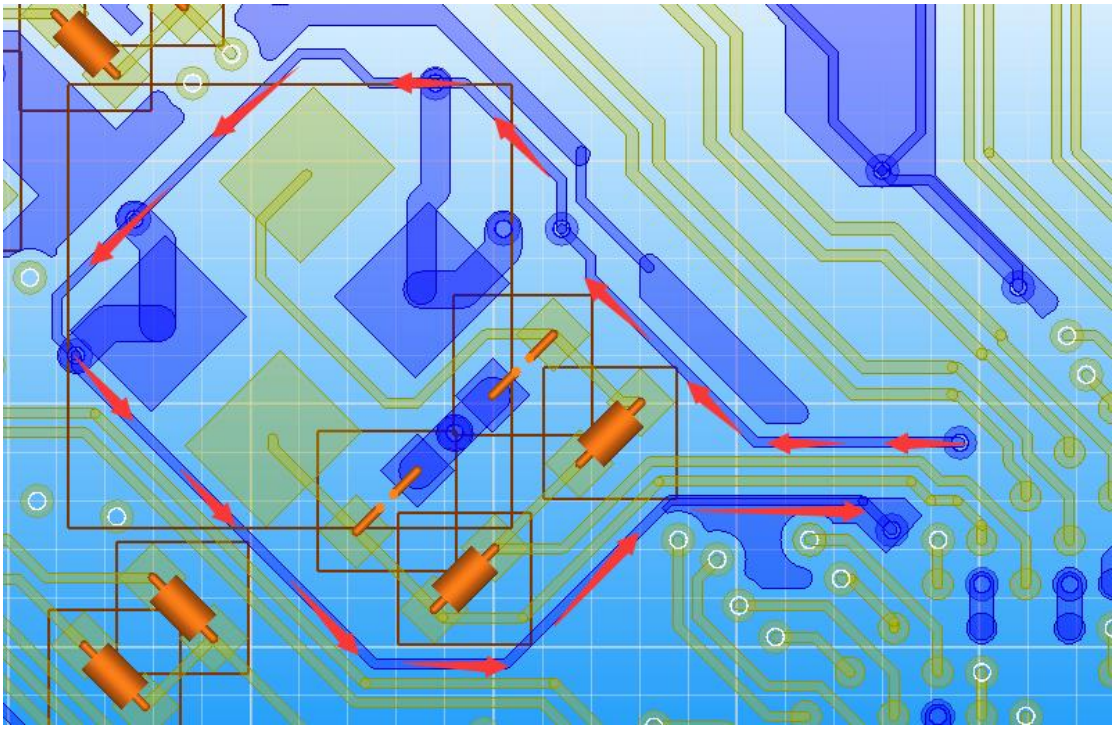

Figure 5: place a guard ring around the crystal

5.2 Trace Bend Geometry

When routing high-speed signals, bends should be minimized. If bends are needed, use 135° bends instead of 90° .

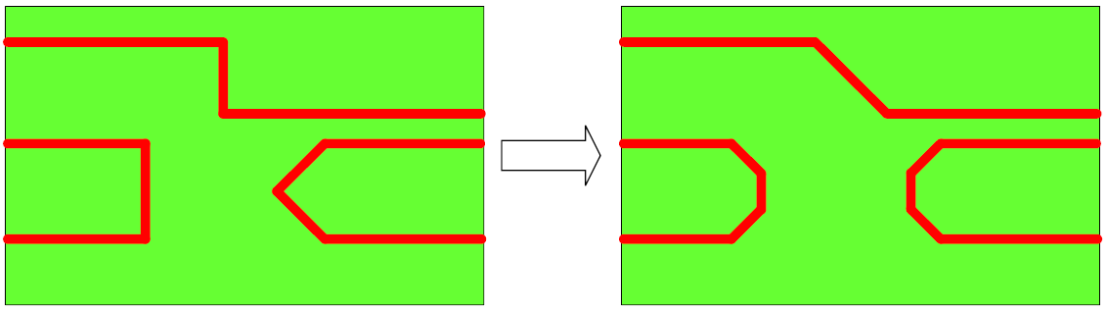

Figure 6: Use 135° Bends instead of 90°

Serpentine traces (also called meander) are often needed when a certain trace length needs to be achieved. For high speed interface , If there is space available, it is suggested to keep a minimum distance of four times the trace width between adjacent copper in a single trace. If its space is tight such as LPDDR3 interface , keep a minimum distance of two times the trace width between adjacent copper in a single trace. The individual segments of the bends should be at least 1.5 times the trace width.

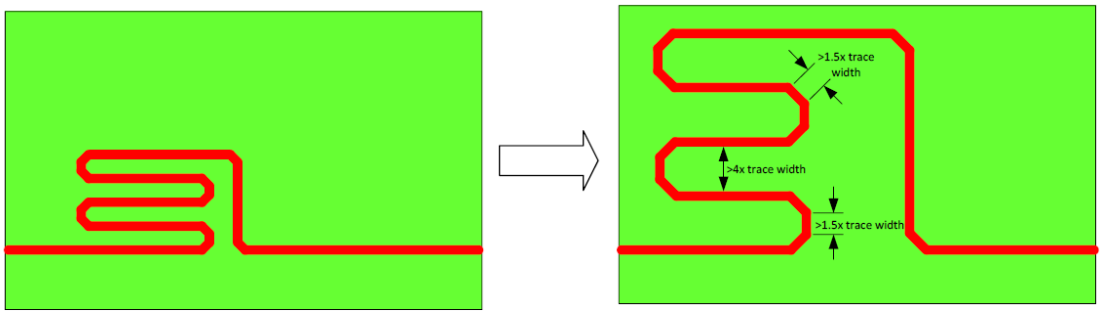

Figure 7: suggested minimum Distance and Segment Length at Bends

5.3 Signal Proximity

Information about the required minimum distance between high-speed signals can be found in section 6. A minimum distance is required in order to minimize crosstalk between traces. The level of crosstalk depends on the distance between two traces and the length in which they are closely routed. Sometimes, bottlenecks can force the routing of traces closer than to what is normally permitted. Try to minimize such areas and enlarge the distance between the signals outside the bottleneck. If there is space available, try to enlarge the distance between the high speed-signals (and between high-speed and low-speed signals) even if the minimum trace separation requirement has been met.

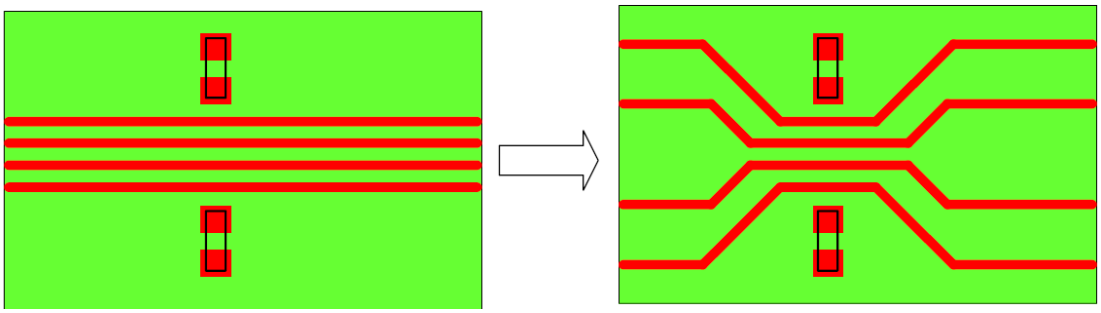

Figure 8: Try to increase Spacing between Traces whenever it is possible

5.4 Trace Stubs

Long stub traces can act as antennas and therefore increase problems complying with EMC standards. Stub traces can also produce reflections which negatively impacts signal integrity. Common sources for stubs are pull-up or pull-down resistors on high speed signals. If such resistors are required, route the signals as a daisy chain.

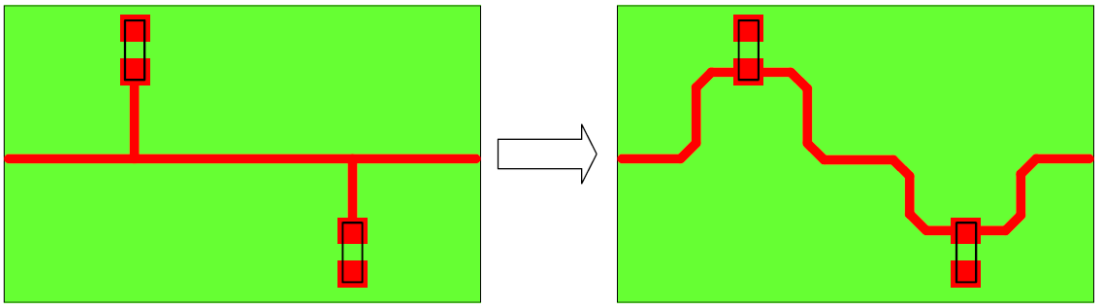

Figure 9: Avoid Stub Traces by Daisy Chain Routing

As a rule of thumb, stubs longer than a tenth of the wavelength should be considered as problematic. The following example shows the calculations on a Gen3 PCIe signal:

$$l_{MAX} \ll \frac{1}{10}\lambda_{MIN} = \frac{v}{10 \cdot f_{MAX}} = \frac{\frac{c}{\sqrt{\varepsilon_r}}}{10 \cdot f_{MAX}} = \frac{\frac{300 \cdot 10^6\, m/_S}{\sqrt{4.5}}}{10 \cdot 4GHz} = 3.5mm$$

Vias can also act as stubs. For example, in a six layer board, when a signal changes from layer 1 to 3 by using a via, the via creates a stub which reaches layer 6. Back-drilling the vias in order to avoid such stubs is a quite expensive technology and one which is not supported by most PCB manufacturers. The only practical solution is to reduce the number of vias in high-speed traces.

5.5 Ground Planes under Pads

The impedance of a trace depends on its width and the distance between trace and reference plane. A wide trace has lower impedance than a thin one with the same distance. The same effect also exists for connector and component pads. A large pad has significantly lower impedance than the trace which is connected to the pad. This impedance discontinuity can cause reflections reduces signal integrity. Therefore, under large connector and component pads, a plane obstruct should be placed.,the area of the plane should decided by means of simulation. In this case, an active reference plane should be placed on another layer. This reference plane's net should be same as the normal reference plane. This reference plane needs to be stitched with vias to the normal reference plane.

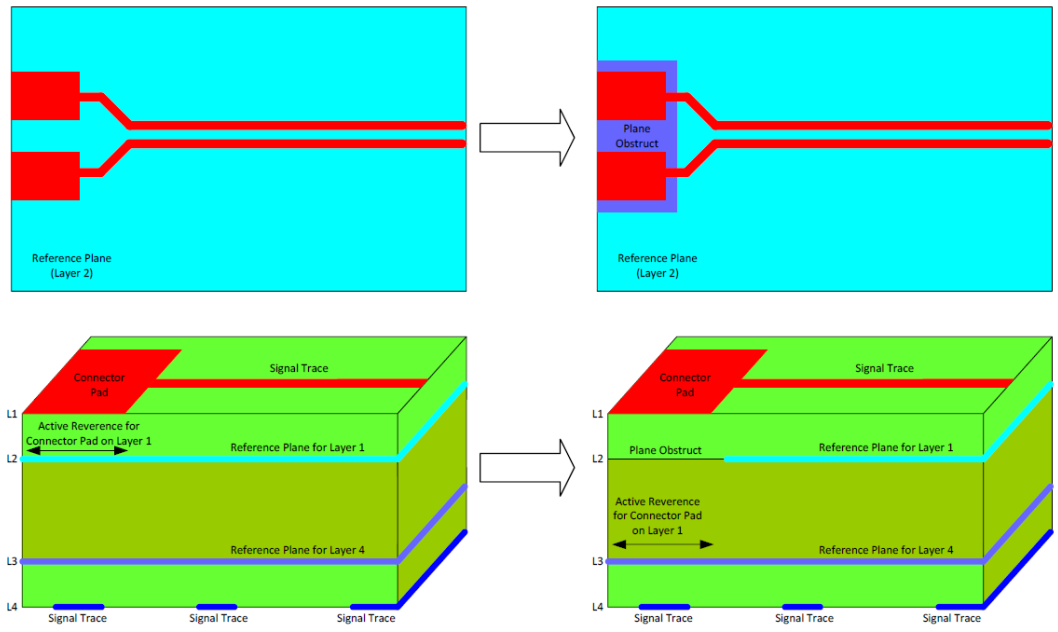

Figure 10: Remove Ground Plane under large Pads

Vias are another source of impedance discontinuity. In order to minimize the effect, the unused pads of vias in inner layers should be removed. This can be done at design time in the CAD tool or by the PCB manufacturer.

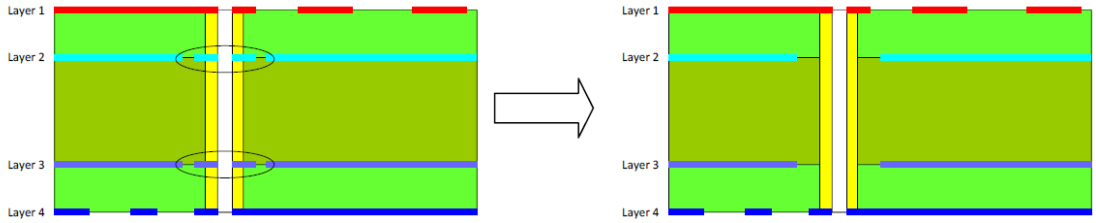

Figure 11: Remove unused Via Pads

5.6 Differential Pair Signals

It is not permitted to place any components or vias between the differential pairs, even if the signals are routed symmetrically. Components and vias between the pairs could lead to EMC compliance problems and create an impedance discontinuity.

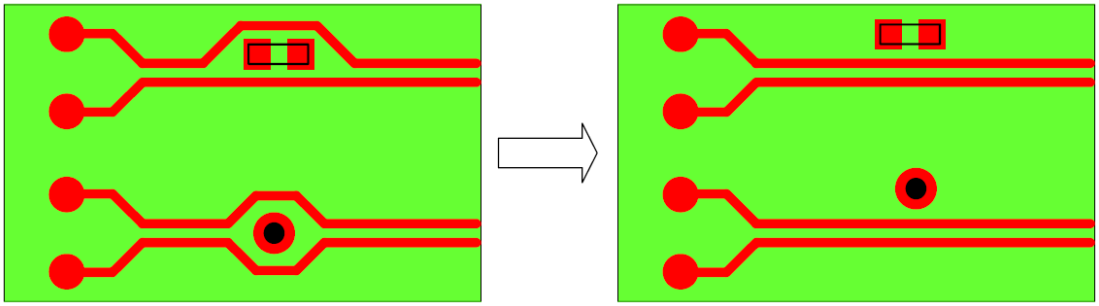

Figure 12: Do not put any Components or Vias between Differential Pairs

Some differential pair high-speed signals require serial coupling capacitors. Place such capacitors symmetrically. The capacitors and the pads create impedance discontinuities. 0201 sized capacitors are preferable, 0402 are acceptable. Do not place larger packages such as 0603 or 0805.

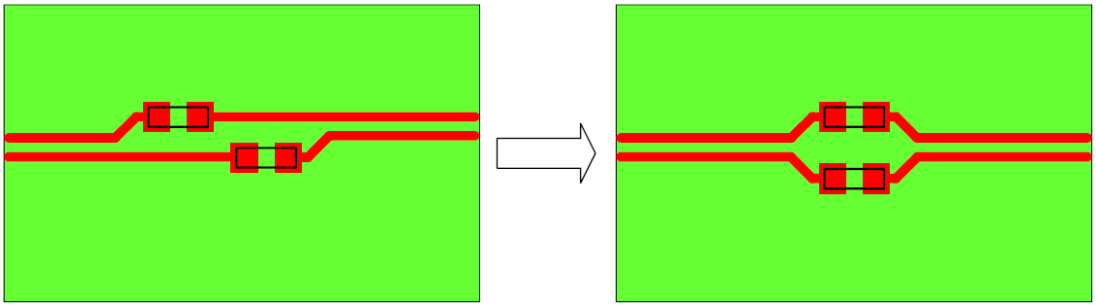

Figure 13: Place Coupling Capacitors symmetrical

Vias introduce a huge discontinuity in impedance. Try to reduce the amount of placed vias to a minimum and place the vias symmetrically.

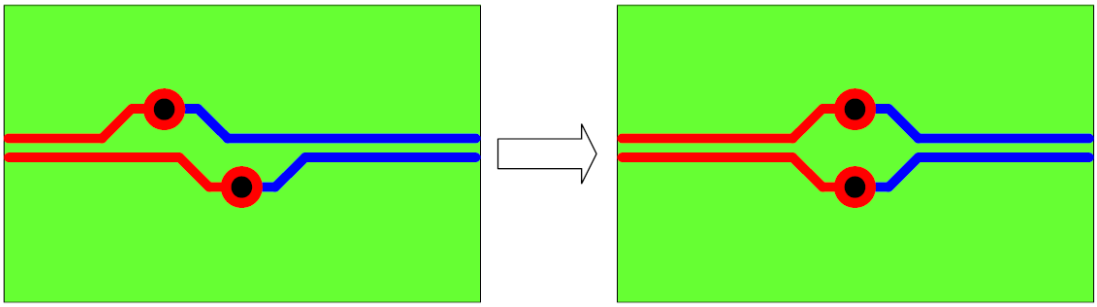

Figure 14: Place Vias symmetrical

In order to meet the impedance requirements of a differential pair, both signal traces need to be routed on the same layer. Add the same amount of vias to the traces.

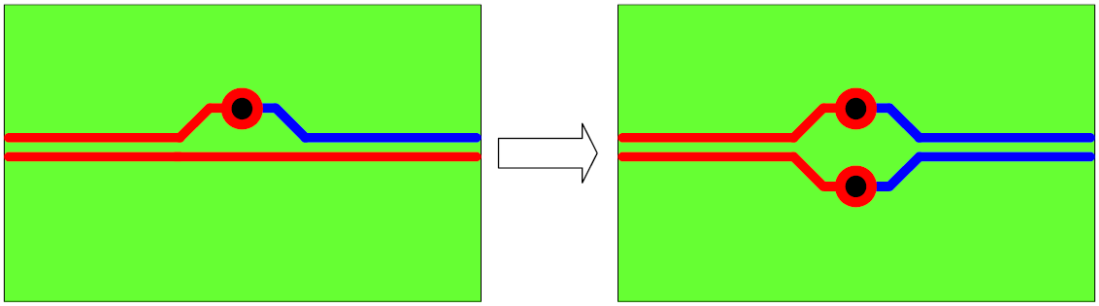

Figure 15: Route Pairs on the same Layer, place same Amount of Vias

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5.7 Length Matching

High-speed interfaces have additional requirements regarding the time of arrival skew between different traces and pairs of signals. For example, in a high speed parallel bus, all data signals need to arrive within a time period in order to meet the setup and hold time requirements of the receiver. The carrier board designer needs to make sure that such permitted skew is not exceeded. In order to meet this requirement, length matching is required. Often, the requirements are given as a maximum time skew.

Differential pair signals often require a very tight delay skew between the positive and negative signal traces. Therefore, length differences need to be compensated for using serpentines (also called meanders). The geometry of serpentine traces need to be carefully chosen in order to reduce impedance discontinuity. The following figure shows the requirements for ideal serpentine traces:

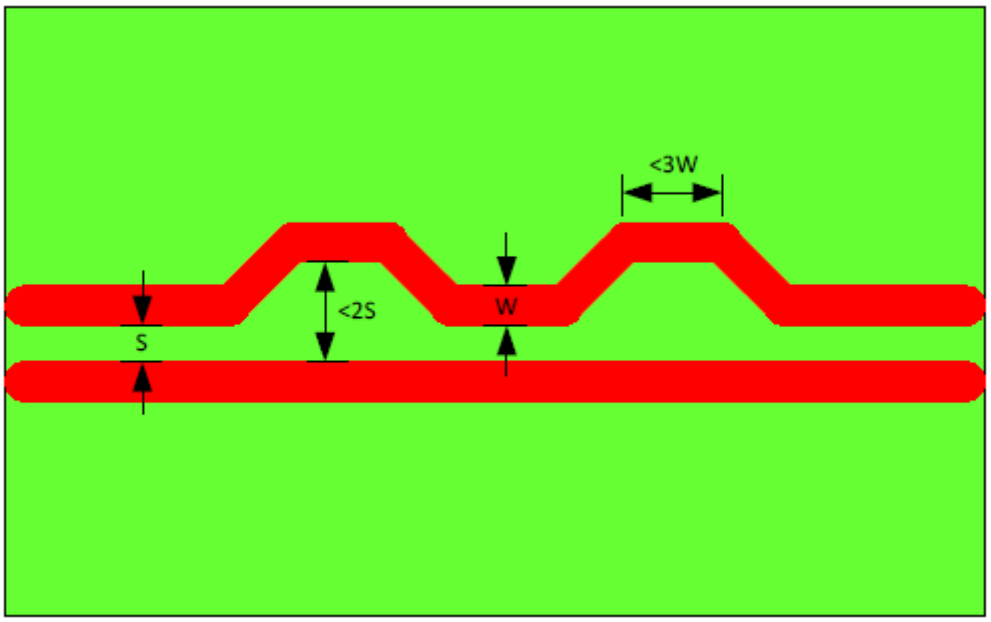

Figure 16: Preferred Serpentine Trace Geometry

5.7.1 package breakout Length Matching

As to RK3399 chip,high speed differential interface such as PCI Express, HDMI, USB ,DP,Mipi，and EDP don't need to do package breakout length mismatching,other location need.Because package and pcb compensate each other in the location of package breakout.

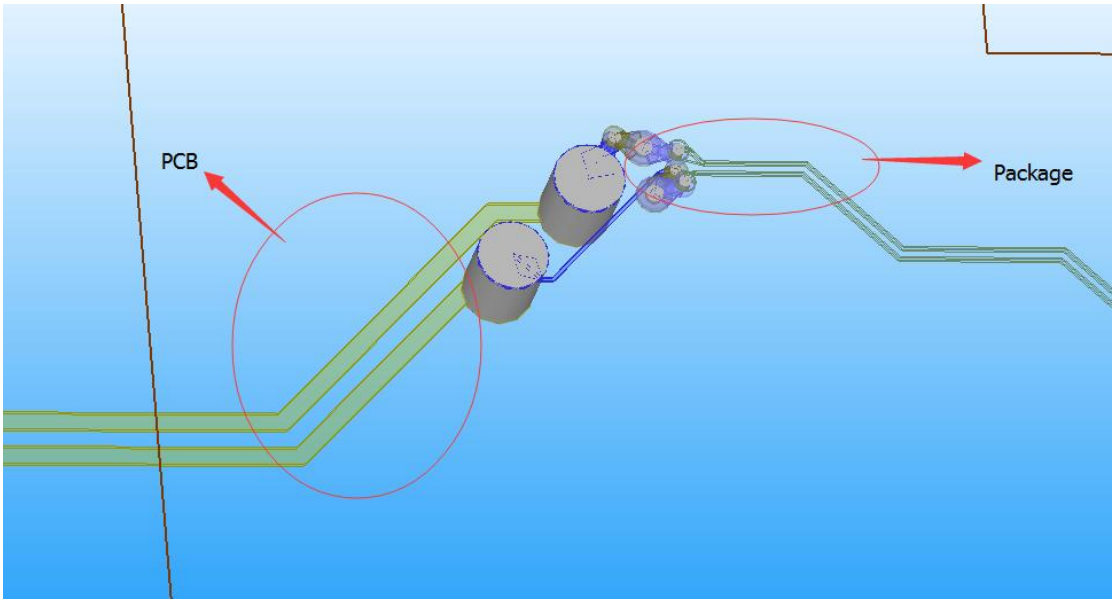

Figure 17: package breakout package and pcb compensate

5.7.2 Length Matching except package breakout

The following figure shows the requirements for length matching except package breakout .

The serpentine traces should be placed at the origin of the length mismatching. This ensures that the positive and negative signal components are propagated synchronously over the major part of the connection.

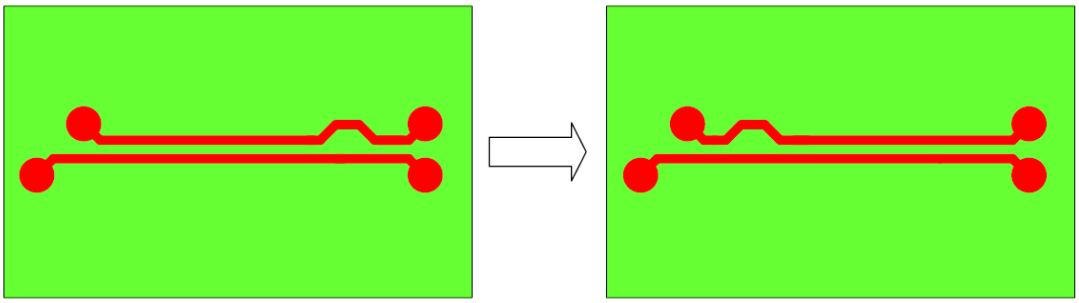

Figure 18: Add Length Correction to the Mismatching Point

Bends are a common source of length mismatching. The compensation should be placed close to the bend with a maximum distance of 15mm.

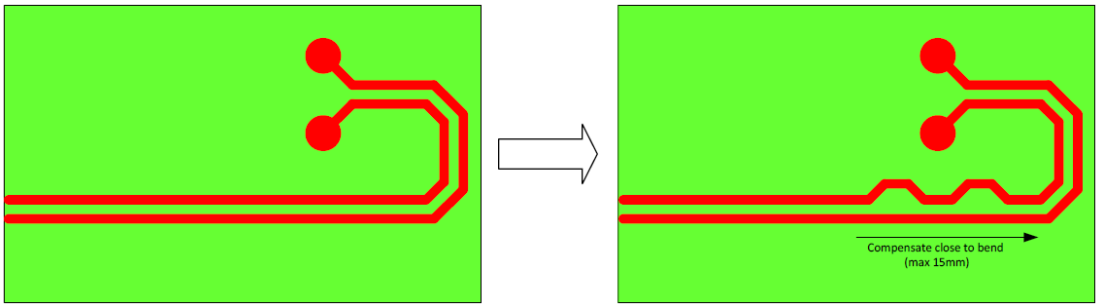

Figure 19: Place Length Compensation close to Bend

Often two bends compensate each other. If the bends are closer than 15mm, no additional compensation with serpentines is necessary. The signals should not propagate asynchronously over a distance greater than 15mm.

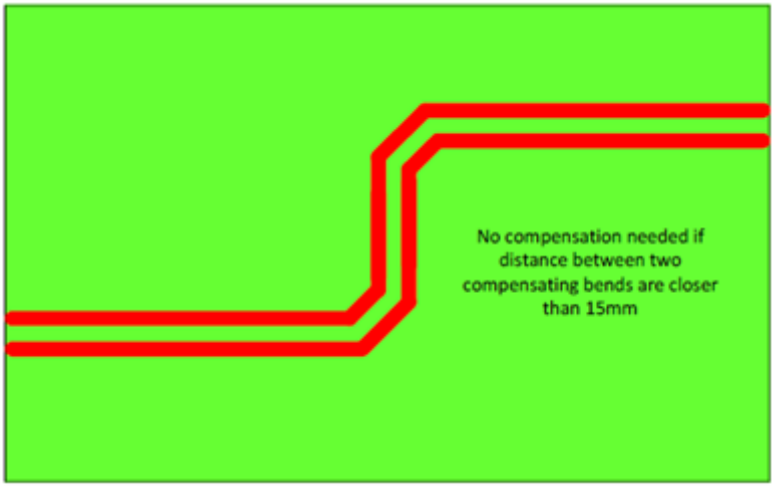

Figure 20: Bends can compensate each other

Each segment of a differential pair connection needs to be matched individually. A connection can be segmented by a connector, serial coupling capacitors or vias. The two bends in the following figure would compensate each other. Since the vias divide the differential pair into two segments, the bends need to be compensated individually. This makes sure that the positive and negative signals are propagated synchronously through the vias. The violation of this rule might need to be checked manually as the DRC may only check the length difference over the whole connection.

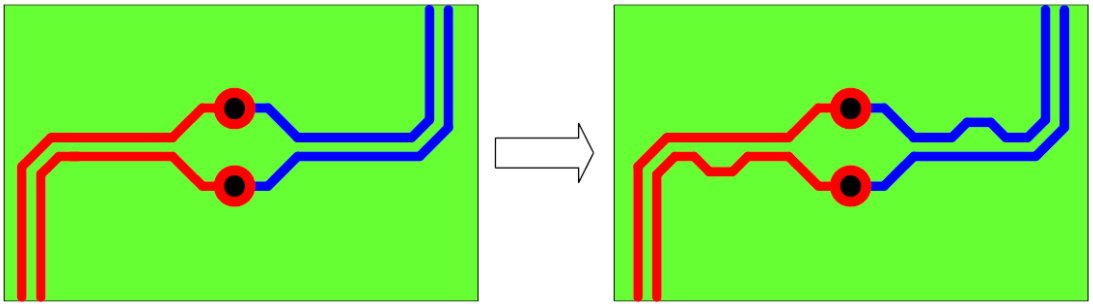

Figure 21: Length Differences need to be compensated in each Segment

The signal speed is not equal for different layers. Since the difference is hard to estimate, it is preferable to route signals on the same layer if they need to be matched. For example, the DDR3display interface requires tight matching between the signal pairs and the clock pair. It is preferable to route all data and clock signals of an DDR3 channel on the same layer.

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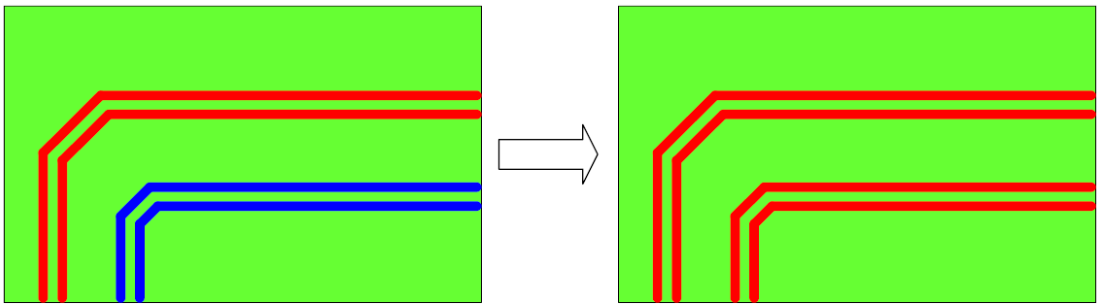

Figure 22: Pairs within same Interface should be routed preferable on same Layer

Please be aware that some CAD tools also accounts the trace length inside a pad to its total length. The following figure shows two layouts which are similar from an electrical point of view. On the left side, the traces inside the capacitor pads do not have equal length. Even though the signals are not using the internal traces, some CAD tools use this as part of the length calculation and show a length difference between the positive and negative signal. In order to minimize the impact of incorrect trace length calculations, ensure that the pad entry is equal for both signals. Similarly, some CAD tools do not take in account the length of vias when calculating the total length. As differential pairs should have the same amount of vias in both traces, the error does not affect the length matching. It can, however, affect calculations for matching two differential pairs or the matching of parallel buses.

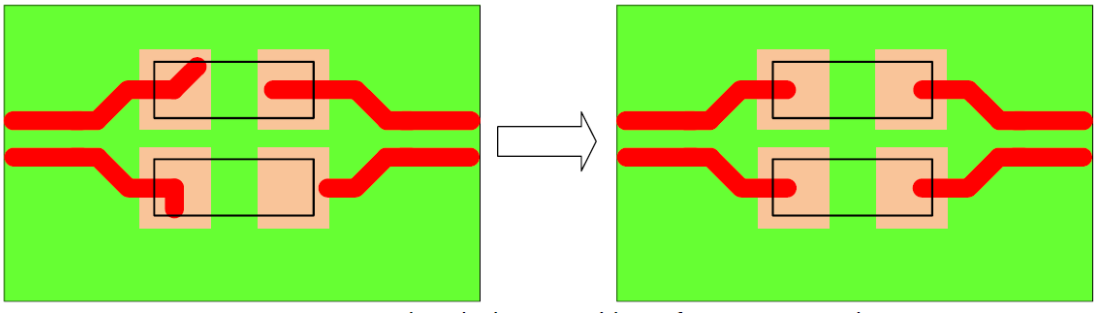

Figure 23: Length Calculation Problem of some CAD Tools

Whenever possible, a symmetric breakout of differential pair signal is preferred in order to avoid the need of serpentine traces.

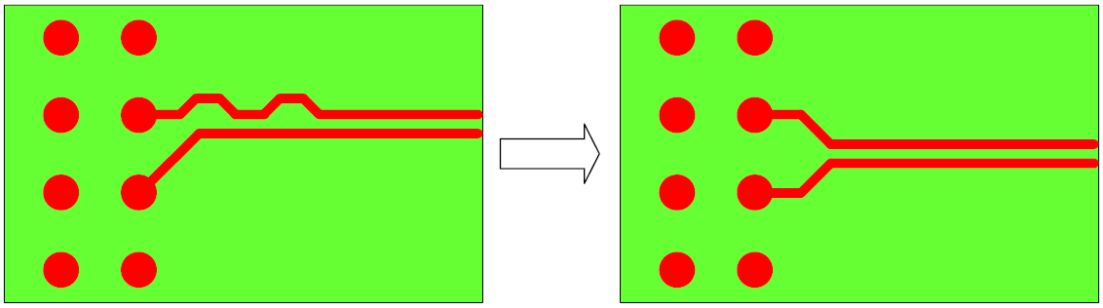

Figure 24: Preferred symmetrical Breakout

If the space between the pads permits, try to add a small loop to the shorter trace. This is the preferred solution for matching the length difference as opposed to creating a serpentine trace.

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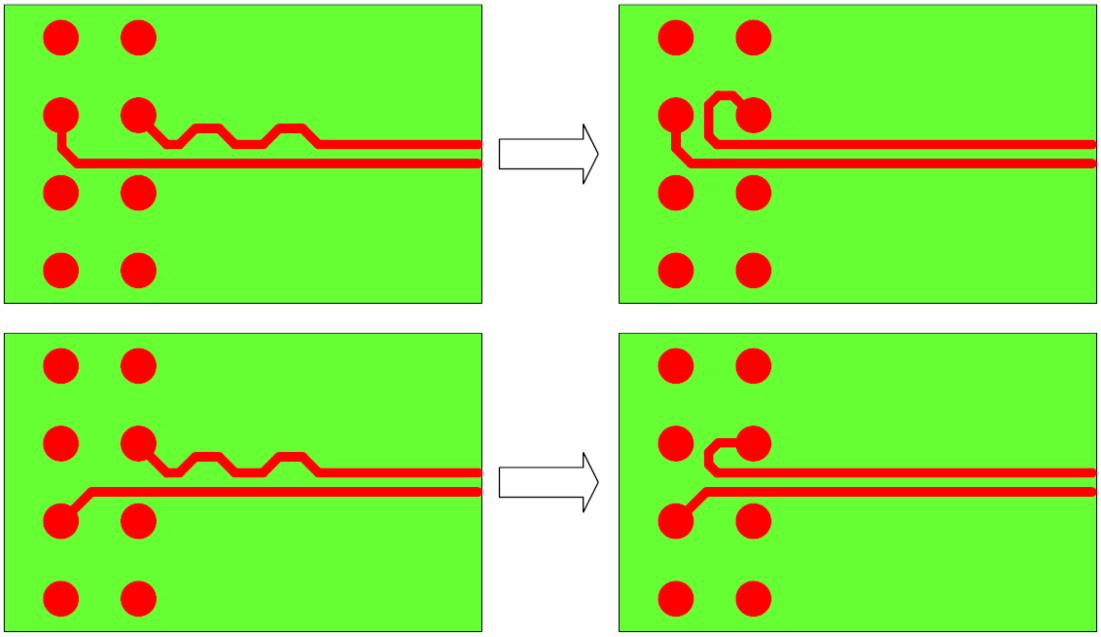

Figure 25: Preferred Breakout of Differential Pairs

5.8 Signal Return Path

An incorrect signal return path is one of the most common sources for noise coupling and EMI problems. The return path of the signal current should always be considered when routing a signal. Power rails and low speed signals take the shortest (lowest resistance) path for the return current. In contrast, the return current of high speed signals tries to follow the signal path. Differential pair signals feature a positive and negative signal trace. Even these signals require a return path which needs to be considered when routing such signals.

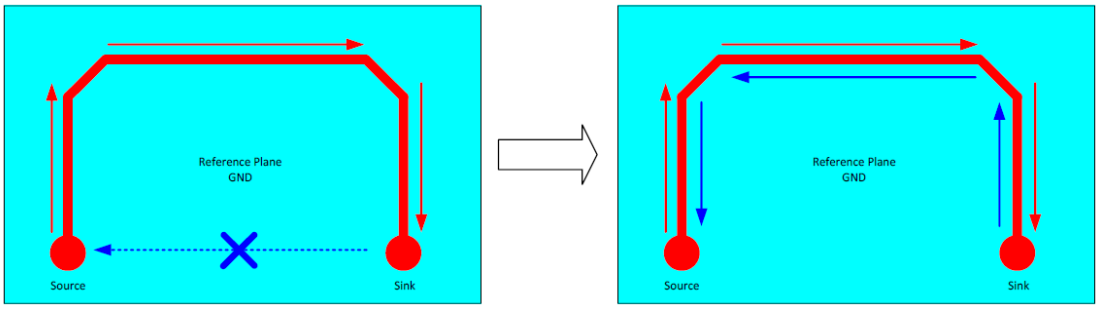

Figure 26: Return Current tries to follow the Signal Path

A signal should not be routed over a spit plane as the return path is not able to follow the signal trace. If a plane is split between a sink and source, route the signal trace around it. If the forward and return paths of a signal are separated, the area between them acts as a loop antenna.

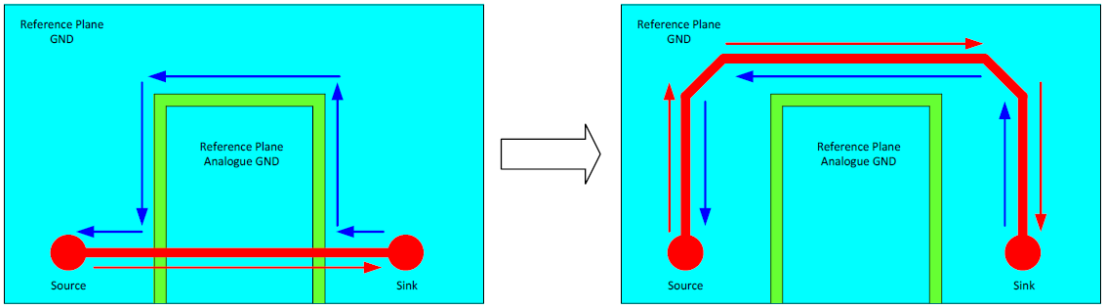

Figure 27: Avoid Routing over Split Planes

If a signal needs to be routed over two different reference planes, a stitching capacitor between the two reference planes is needed. The capacitor allows the return current to travel from one reference plane to the other. The capacitor should be placed close to the signal path in order to keep the distance between forward and return path small. A good value for the stitching capacitor is between 10nF and 100nF.

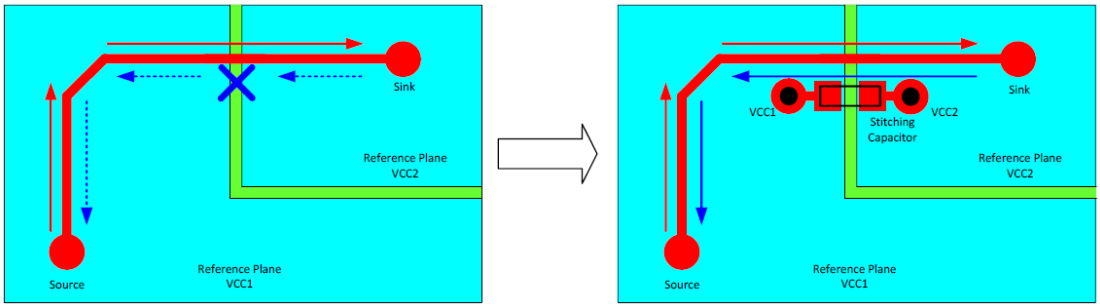

Figure 28: Stitching Capacitor needed when routed over Split Planes

Plane obstructions and plane slots should be avoided in general. Try to avoid routing signals over such obstructions. If unavoidable, stitching capacitors should be used to minimize the problems created by a separated return path.

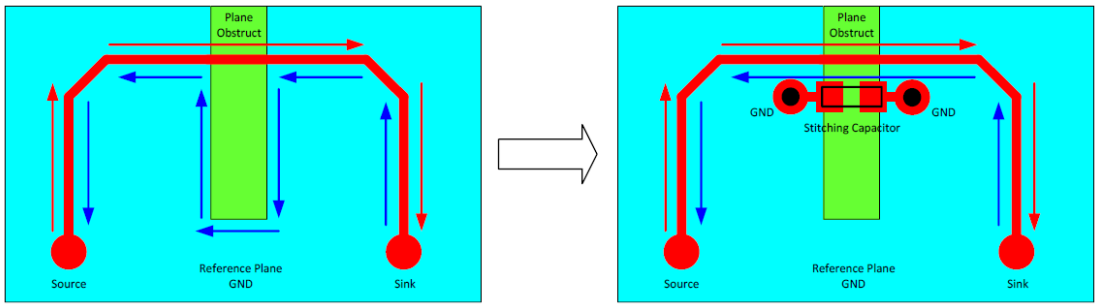

Figure 29: Stitching Capacitor needed when routing over Plane Obstructs

Voids in reference planes can result when placing vias close together. Be aware of such voids when routing high-speed signals. Try to avoid large void areas by ensuring adequate separation between vias. Sometimes, it is better to place fewer ground and power vias in order to reduce via voids.

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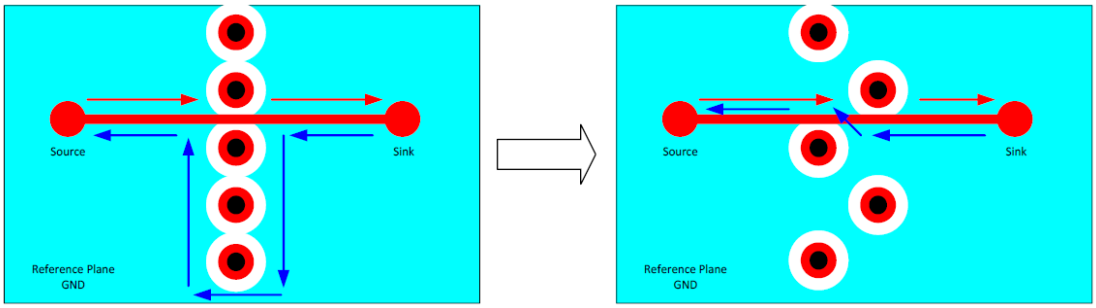

Figure 30: Avoid Via Plane Voids

The return path needs to be considered at the source and sink of a signal. The left figure below shows a bad example. As there is only one single ground via on the source side, the return current cannot travel back over the reference ground plane as intended. The return path for the current is the ground connection on the top layer instead. The problem is that the impedance of the signal trace is calculated as referenced to the ground plane and not to the ground trace on the top layer. Therefore, it is necessary to place ground vias at the source and sink side of the signal. This permits the return current to travel back on the ground plane.

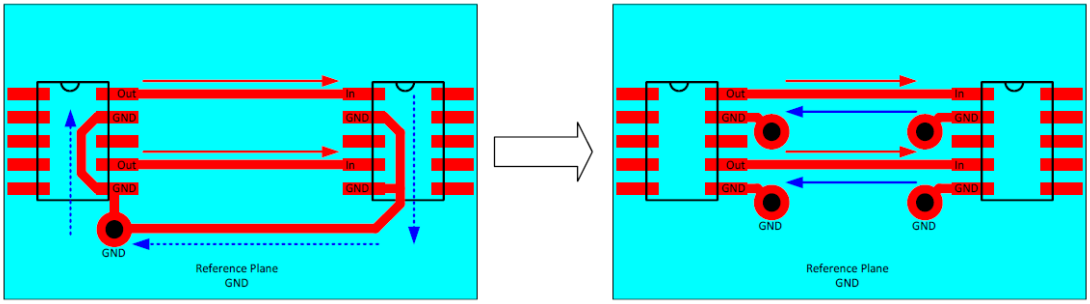

Figure 31: Consider Return Path when placing Ground Vias

When a signal trace uses a power plane as reference, the signal needs to be able to travel back over the power plane. In the source and sink, the signals are referenced to ground. In order to change the reference to the power plane, stitching capacitors at the sink and source are needed. If the sink and source are using the same power rail for their supply, the bypass capacitors can act as stitching capacitors if they are placed close to the signal entry/exit point. A good value for the stitching capacitor is between 10nF and 100nF.

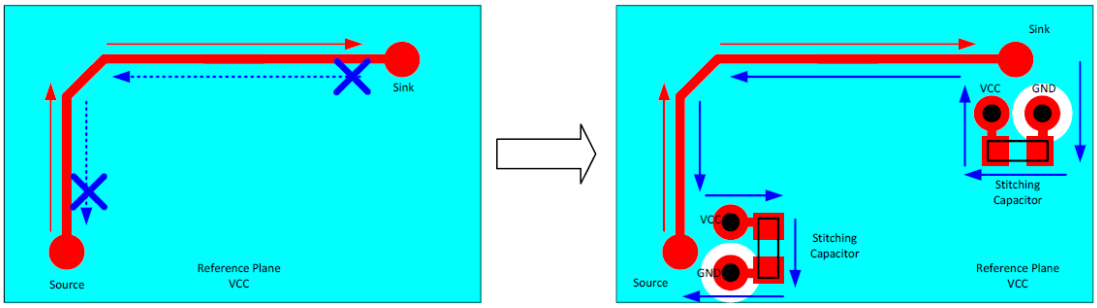

Figure 32: Add Stitching Capacitors when using Power Plane as Reference

If a signal trace switches layer and therefore, also the reference ground plane, stitching vias should to be added close to the layer change vias. This allows the return current to change ground plane. For differential signals, switching ground vias should be placed symmetrically.

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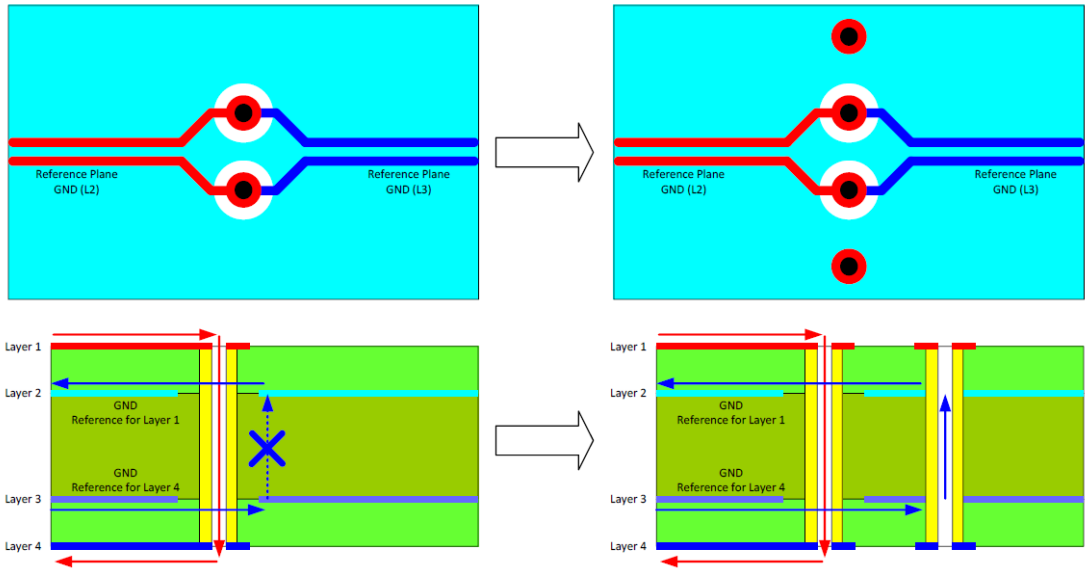

Figure 33: Place Stitching Vias when Signal changes Ground Reference

If a signal trace switches to a layer which has a different net as reference (e.g. from ground reference to power plane reference), stitching capacitors are required. This allows the return current to flow from the ground plane through the stitching capacitor to the power plane. Stitching capacitor placement and routing should be symmetrical for differential pair signals.

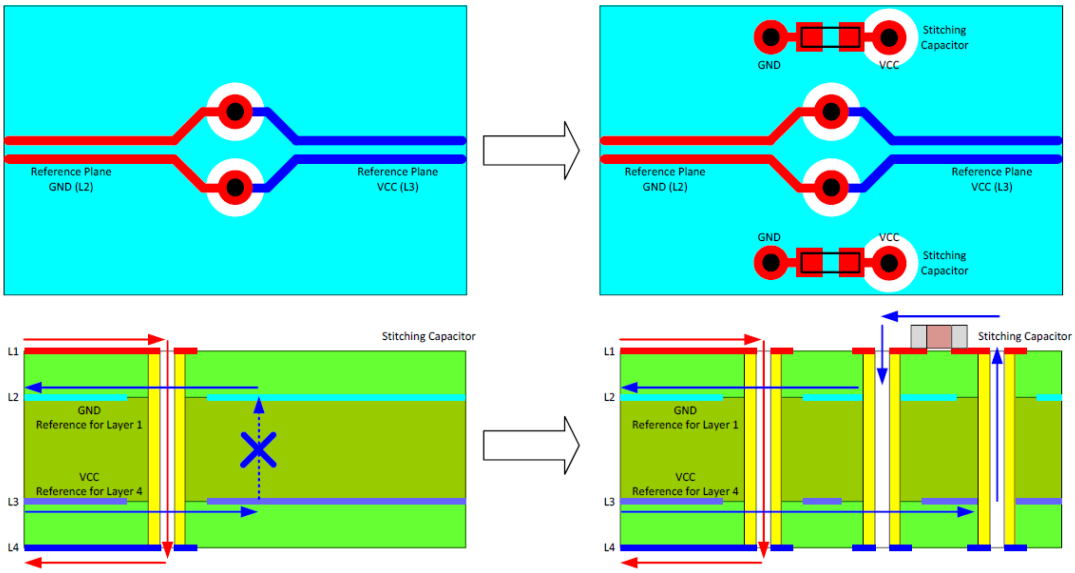

Figure 34: Place Stitching Capacitors when changing Signal Reference Plane

Avoid routing high-speed signals on the edge of reference planes or close to PCB borders. Otherwise, this can adversely affect the trace impedance.

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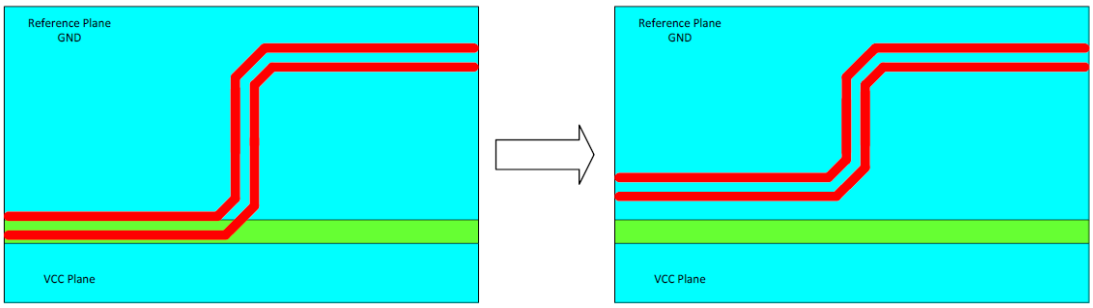

Figure 35: Do not route High Speed Signals at Plane and PCB borders

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6 Layout Requirements of Interfaces

Depending on the type of interface, there are different layout requirements available. This section provides an overview of the major interfaces that can be found on RK3399 chip.

The differential pair signals normally distinguish between two different length matching requirements. The first requirement is the maximum intra-pair skew. This is the maximum allowed length differences between the positive and negative signal of the pairs. As described in section 5, not only should the overall length be matched, but also the length within a section of the signal should be corrected. It is important that the positive and negative signal components are propagated synchronously. Only if these signals are synchronous, their fields are compensated and the electromagnetic radiation is reduced.

The second length matching requirement is the maximum allowed skew between the clock and signal pairs or between different pairs of the same interface. Some of the interfaces (e.g. PCIe, EDP, DP,and USB3.0) are recovering the clock signal out of the data signals. Therefore, the matching between the clock and data signals can be quite relaxed. Do not try to overmatch such interfaces since it is really not required and the additional meander just introduces other signal quality problems. On the other hand there are interfaces which do not have an embedded clock signal (e.g. Mipi interface). Please route these signals very carefully. The length matching between the clock and data signals needs to be met.

Vias introduce a major discontinuity of the impedance and can create signal stubs. Therefore, the amount of vias should be kept as low as possible.

6.1 PCI Express

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<4ps
Max inter-pair skew	<1.6ns
Maximum signal line length (coupled traces) TX and RX	<14 inches
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
Minimum pair to pair spacing	>3 times the width of the trace. Try to increase Spacing between pairs whenever it is possible.
Length matching between reference clock differential pairs REFCLK+ and REFCLK-	<4ps

(intra-pair)	
The minimum spacing between PCIE and other Signals	At least 3 times the width of PCIE trace.
Maximum allowed via	4

Note:

It is suggest that PCIE signals route together .Don't have any other signals and via within PCIE signals .

6.2 USB

The layout requirement for USB interfaces depends on the version that needs to be supported. Up to USB 2.0, the interface was consisting of a single bidirectional data signal pair. The USB 3.0 standard introduces two additional data signal pairs for the Super Speed link. These two pairs are running at 5 Gbit/s .

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length on carrier board	<6 inches
Maximum allowed via	6

6.2.1.2 USB 3.0 Signals

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length skew between RX and TX data pairs	<1.6ns
Max trace length on carrier board	<6 inches
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
Minimum pair to pair spacing	>3 times the width of the trace. Try to increase Spacing between pairs whenever it is possible.

The minimum spacing between USB and other Signals	At least 3 times the width of USB trace.
Maximum allowed via	4

Note:

It is suggest that USB signals route together .Don't have any other signals and via within USB signals .

6.3 HDMI

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length skew between clock and data pairs	<80ps
Max trace length on carrier board	<9.8 inches
Minimum pair to pair spacing	>3 times the width of the trace. Try to increase Spacing between pairs whenever it is possible.
The minimum spacing between HDMI and other Signals	At least 3 times the width of HDMI trace.
Maximum allowed via	4

Note:

It is suggest that HDMI signals route together .Don't have any other signals and via within HDMI signals .

6.4 EDP

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length on carrier board	<6 inches

Minimum pair to pair spacing	>3 times the width of the trace.Try to increase Spacing between pairs whenever it is possible.
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
The minimum spacing between EDP and other Signals	At least 3 times the width of EDP trace.
Maximum allowed via	4

Note:

It is suggest that EDP signals route together .Don't have any other signals and via within EDP signals .

6.5 Display Port

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<4ps
Maximum signal line length (coupled traces)	<6 inches
Minimum pair to pair spacing	>3 times the width of the trace.Try to increase Spacing between pairs whenever it is possible.
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
The minimum spacing between Display Port and other Signals	At least 3 times the width of Display Port trace.
Maximum allowed via	4

Note:

It is suggest that Display Port signals route together .Don't have any other signals and via within Display Port signals .

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6.6 Mipi

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length skew between clock and data pairs	<7ps
Max trace length	<7.2 inches
Maximum allowed via	Minimize the number of via in each lane
Minimum pair to pair spacing	>3 times the width of the trace.Try to increase Spacing between pairs whenever it is possible.
The minimum spacing between Mipi and other Signals	At least 3 times the width of Mipi trace.

Note:

It is suggest that Mipi signals route together .Don’t have any other signals and via within Mipi signals .

6.7 EMMC

EMMC V5.0/V5.1

Parameter	Requirement
Trace Impedance	50Ω ±10% single ended
Max skew between data signal and clock	<20ps
Max trace length	<3.93 inches
The minimum spacing of EMMC Signals	At least 2 times the width of EMMC trace.
The minimum spacing between EMMC and other Signals	At least 3 times the width of EMMC trace.

Note:

It is suggest that EMMC signals route together .Don’t have any other signals and via within EMMC signals .

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6.8 SPI

Parameter	Requirement
Trace Impedance	50Ω ±10% single ended
Max skew between data signal and clock	<100ps
Max trace length	<5 inches

6.9 UART

Parameter	Requirement
Trace Impedance	50Ω ±10% single ended
Max skew between data signals	<100ps
Max trace length	<5 inches

6.10 SDIO

Parameter	Requirement
Trace Impedance	50Ω ±10% single ended
Max skew between data signal and clock	<20ps
Max trace length	<3.93 inches
The minimum spacing of SDIO Signals	At least 2 times the width of SDIO trace.

6.11 USIC

Parameter	Requirement
Trace Impedance	50Ω ±10% single ended
Max skew between USIC_DATA and USIC_STROBE	<5ps
Max trace length	<3.93 inches
USIC_DATA and USIC_STROBE Spacing	≥3 times the width of the trace

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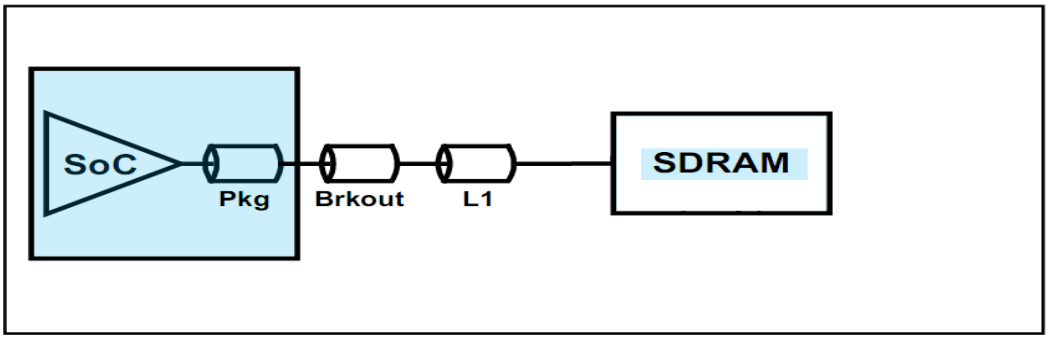
6.12 LPDDR3

This requirements covers the layout guidelines required to LPDDR3 Memory Down at 800 MT/s.

LPDDR3 all signals include Data,Command,clk and control Signals have the same Routing Topology :



Data(DQ/DM/DQS) sigal

Parameter	Definition
Signal Group	DQ， DM， DQS
Target Impedance (Z0:DQ; Zdiff: DQS)	DQ: 50 Ohm ± 10%, DQS: 100 Ohm ± 10% , DM: 50 Ohm ± 10%
DQS Routing Trace Width and Spacing within pair	PCB stack-up dependent
DQ Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
DQS to DQ Spacing within same Byte Group	≥2 times the width of the trace
Byte Group to Byte Group Spacing, Data to Other Signals Spacing	≥2 times the width of the trace
Max intra-pair skew of DQS	1ps
Max skew between DQ/DM and DQS	5ps

Note:

DQ group A include：（DATA0—DATA7，DQM0，DQS0P/ DQS0M）

DQ group B include：（DATA8—DATA15，DQM1，DQS1P/ DQS1M）

DQ group C include：（DATA16—DATA23，DQM2，DQS2P/ DQS2M）

DQ group D include：（DATA24—DATA31，DQM3，DQS3P/ DQS3M）

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The 5ps is the max skew inside DQ groups.It is no the requirement between DQ groups.Because max skew between CLK and DQS is 150ps,so the max skew between DQ groups is 150ps too.

CLK singal

Parameter	Definition
Signal Group	CLK
Target Impedance (Diff Z0)	100 Ohm ± 10%
CLK Routing Trace Width and Spacing within pair	PCB stack-up dependent
CLK Routing Spacing to other Signals	≥3 times the width of the trace
Max intra-pair skew of CLK	1ps
Max skew between CLK and DQS	150ps

Control (CTL) Signal

Parameter	Definition
Signal Group	CSn，CKE
Target Impedance (Z0)	50 Ohm ± 10%
CTL Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥3 times the width of the trace
Max skew between CTL and CLK	5ps

Command (CMD) Signal

Parameter	Definition
Signal Group	LPDDR3_A[0:9]
Target Impedance (Z0)	50 Ohm ± 10%
CA Routing Trace Width and Spacing	Width : PCB stack-up dependent Spacing : ≥3 times the width of the trace

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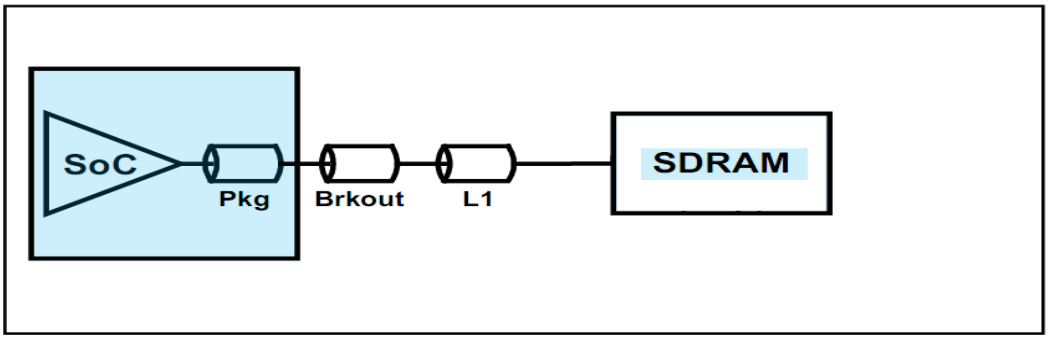
Max skew between CMD and CLK	5ps

6.13 DDR3

This requirements covers the layout guidelines required to DDR3 Memory Down at 800 MT/s.

Data(DQ/DM/DQS) sigal

Data Signal Routing Topology:



Parameter	Definition
Signal Group	DQ，DM，DQS
Target Impedance (Z0:DQ; Zdiff: DQS)	DQ: 50 Ohm ± 10%, DQS: 100 Ohm ± 10% , DM: 50 Ohm ± 10%
DQS Routing Trace Width and Spacing within pair	PCB stack-up dependent
DQ Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
DQS to DQ Spacing within same Byte Group	≥2 times the width of the trace
Byte Group to Byte Group Spacing, Data to Other Signals Spacing	≥2 times the width of the trace
Max intra-pair skew of DQS	1ps
Max skew between DQ /DM and DQS	5ps

Note:

DQ group A include：（DATA0—DATA7，DQM0，DQS0P/ DQS0M）

DQ group B include：（DATA8—DATA15，DQM1，DQS1P/ DQS1M）

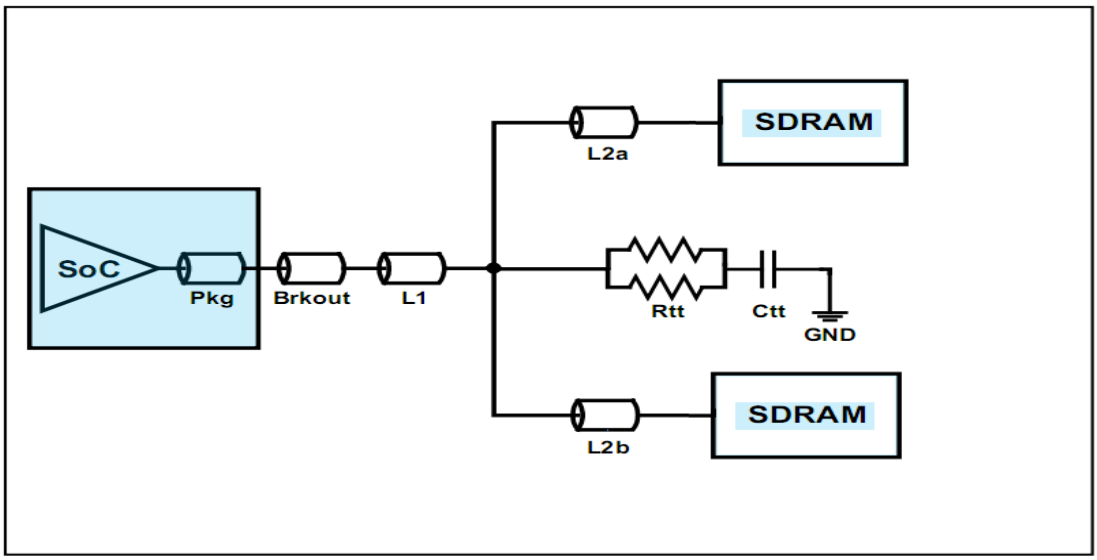
DQ group C include：（DATA16—DATA23，DQM2，DQS2P/ DQS2M）

DQ group D include：（DATA24—DATA31，DQM3，DQS3P/ DQS3M）

The 5ps is the max skew inside DQ groups.It is no the requirement between DQ groups.Because max skew between CLK and DQS is 150ps,so the max skew between DQ groups is 150ps too.

CLK singal

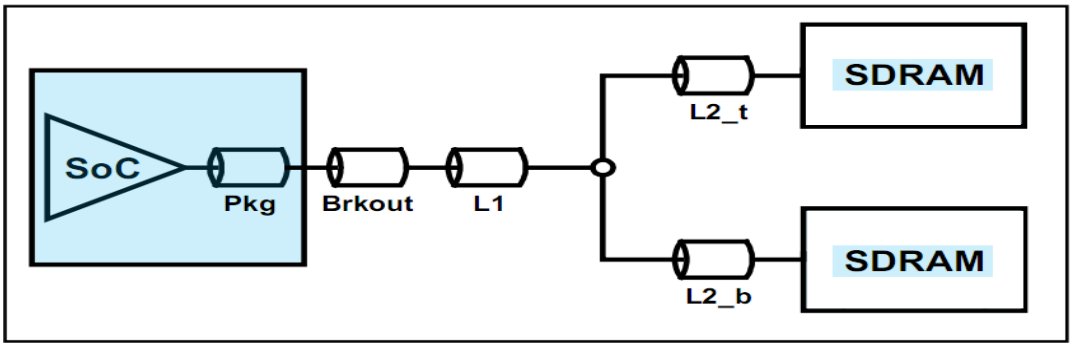
CLK Signal Routing Topology:



Parameter	Definition
Signal Group	CLK
Target Impedance (Diff Z0)	100 Ohm ± 10%
CLK Routing Trace Width and Spacing within pair	PCB stack-up dependent
CLK Routing Spacing to other Signals	≥2 times the width of the trace
Max intra-pair skew of CLK	1ps
Max skew between CLK and DQS	150ps
L2a, L2b	length match L2a and L2b within 1 ps

Control (CTL) Signal

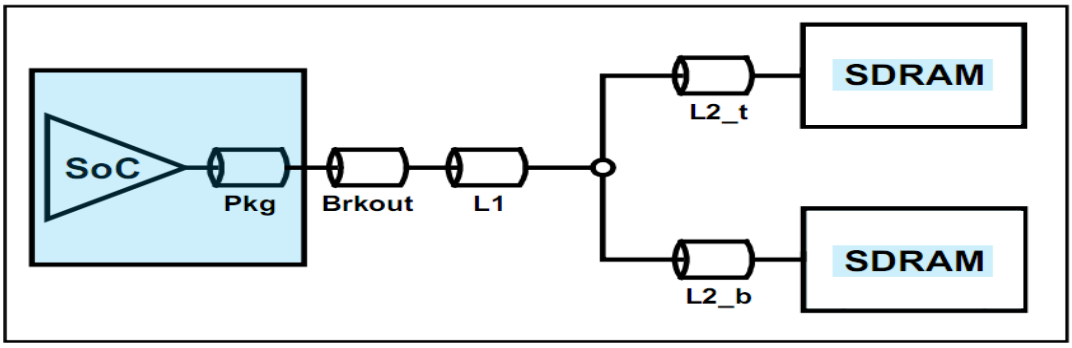
Control Signal Routing Topology:



Parameter	Definition
Signal Group	CSB，CKE，ODT
Target Impedance (Z0)	50 Ohm ± 10%
CTL Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CTL and CLK	10ps
L2a, L2b	length match L2a and L2b within 1 ps

Command (CMD) Signal

Command Signal Routing Topology:



Parameter	Definition
Signal Group	DDR3_A[0:15], DDR3_CASB, DDR3_RASB, DDR3_WEB
Target Impedance (Z0)	50 Ohm ± 10%
CA Routing Trace Width and Spacing	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CMD and CLK	10ps
L2a, L2b	length match L2a and L2b within 1 ps

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