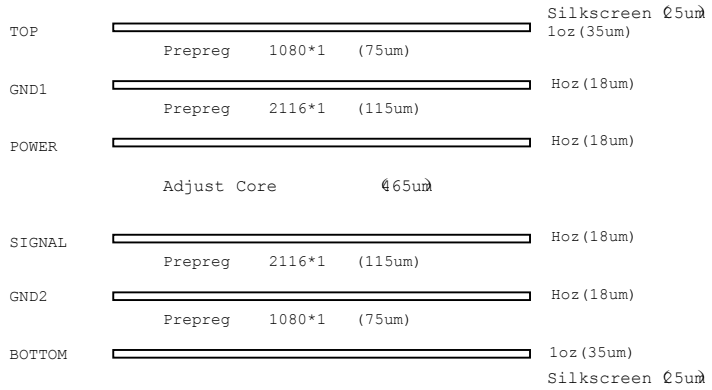
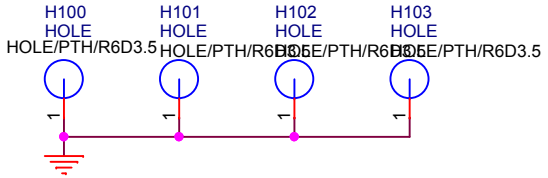
RK3399_Rock960_V2.1

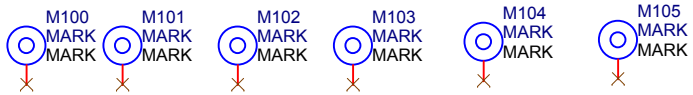
CONTENT INDEXING

6 LAYERS PCB STACK (PCB=1.6mm)



Note:
器件参数说明
1:如果Value为DNP,则此器件暂时不贴。
2:如果Option有DNP,则此器件预留先不贴。





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Change List

Version	Date	Author	Change Note	Approved
V1.0	201708	Charlie	First edition	

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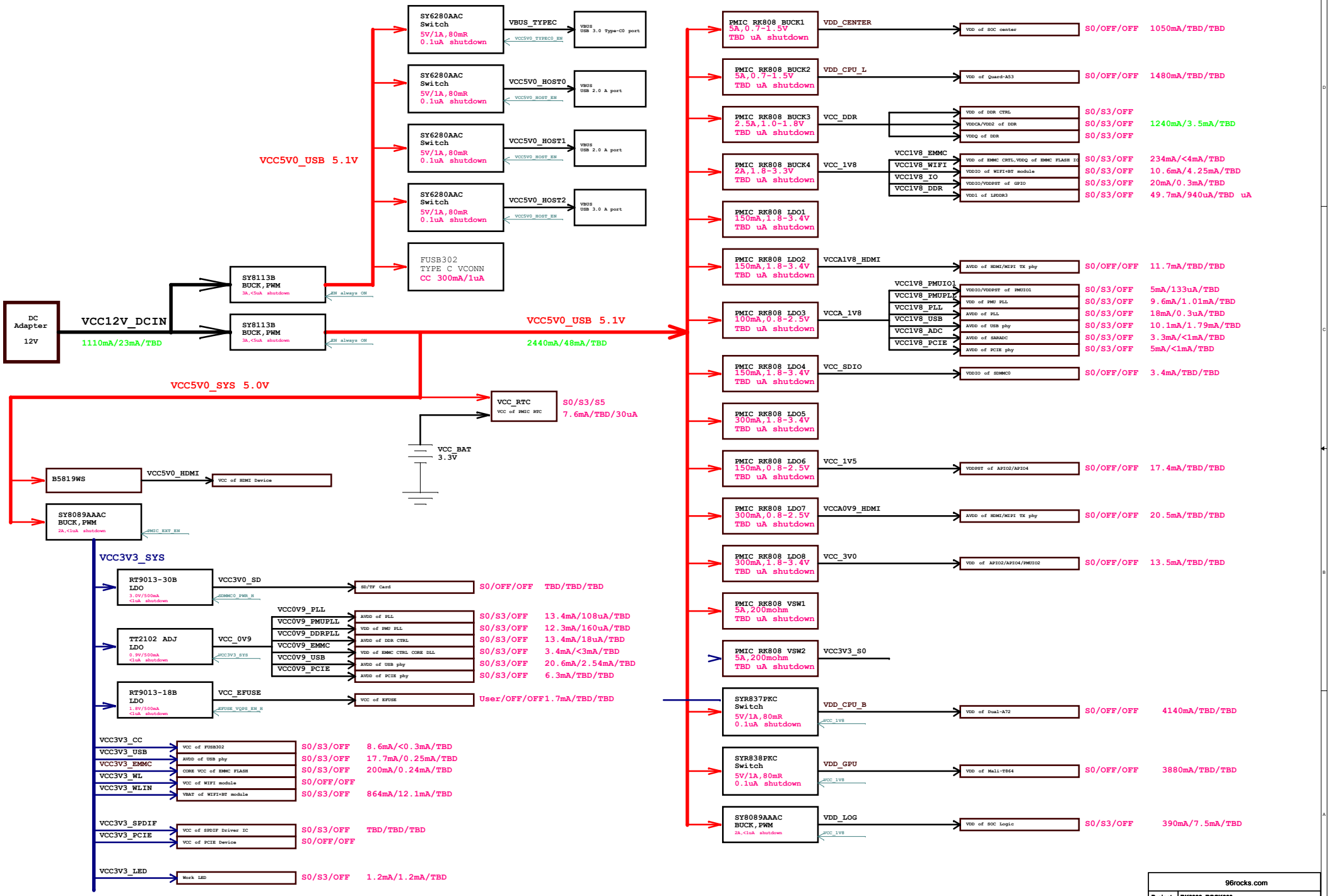
RK3399 POWER DIAGRAM



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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5		VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECTOR	
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	

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Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmu1830_gpio1abcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_SYS	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLDO4

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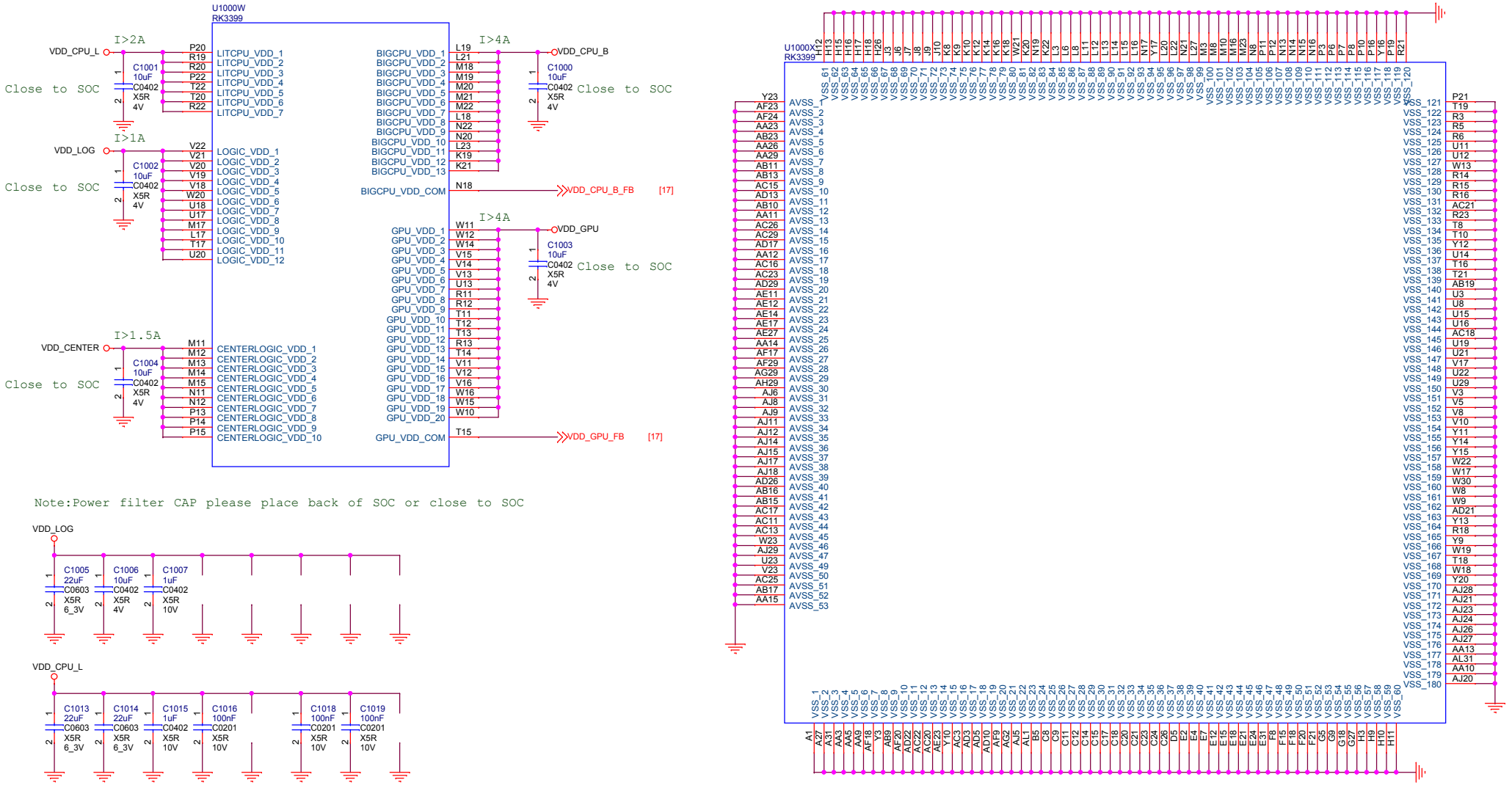
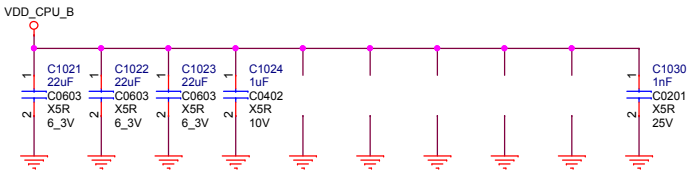
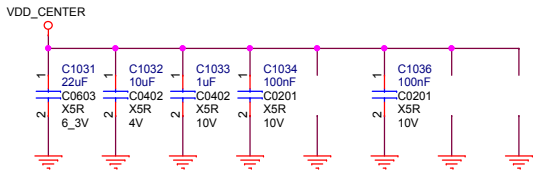
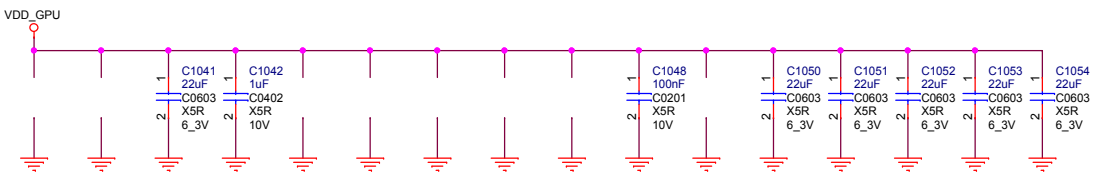


Note:Power filter CAP please place back of SOC or close to SOC







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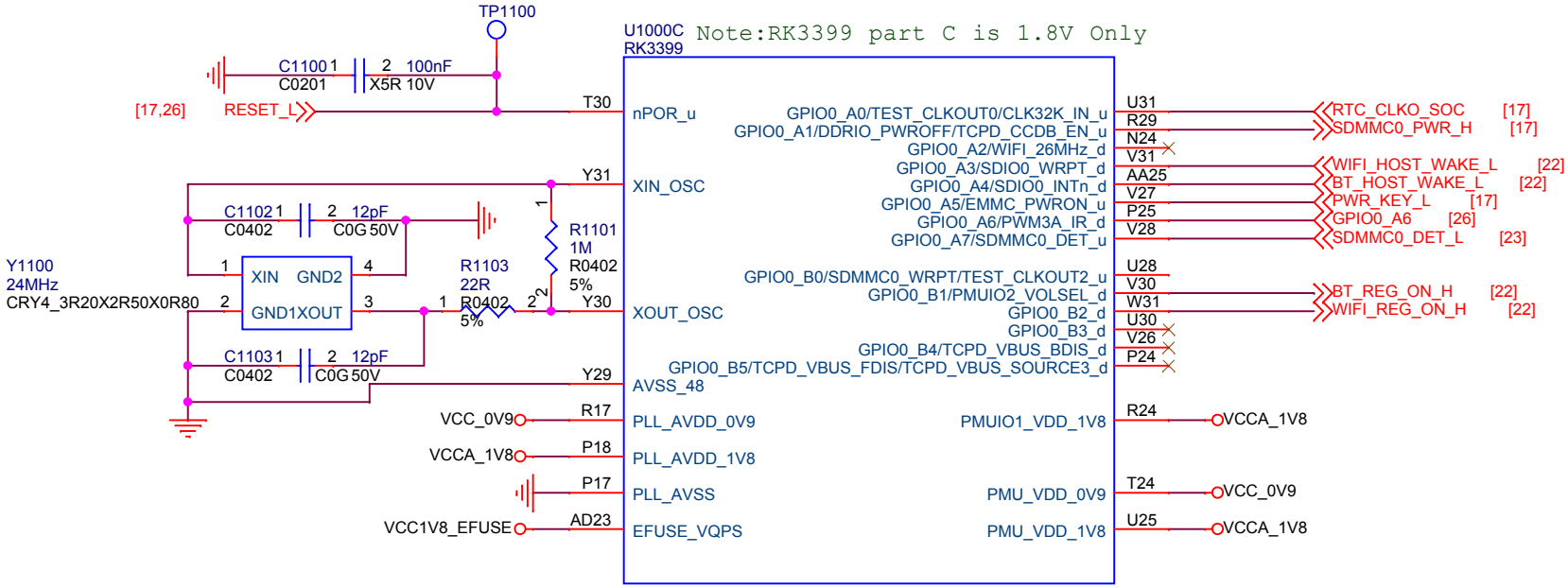

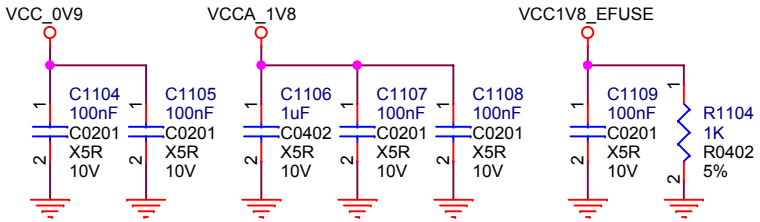

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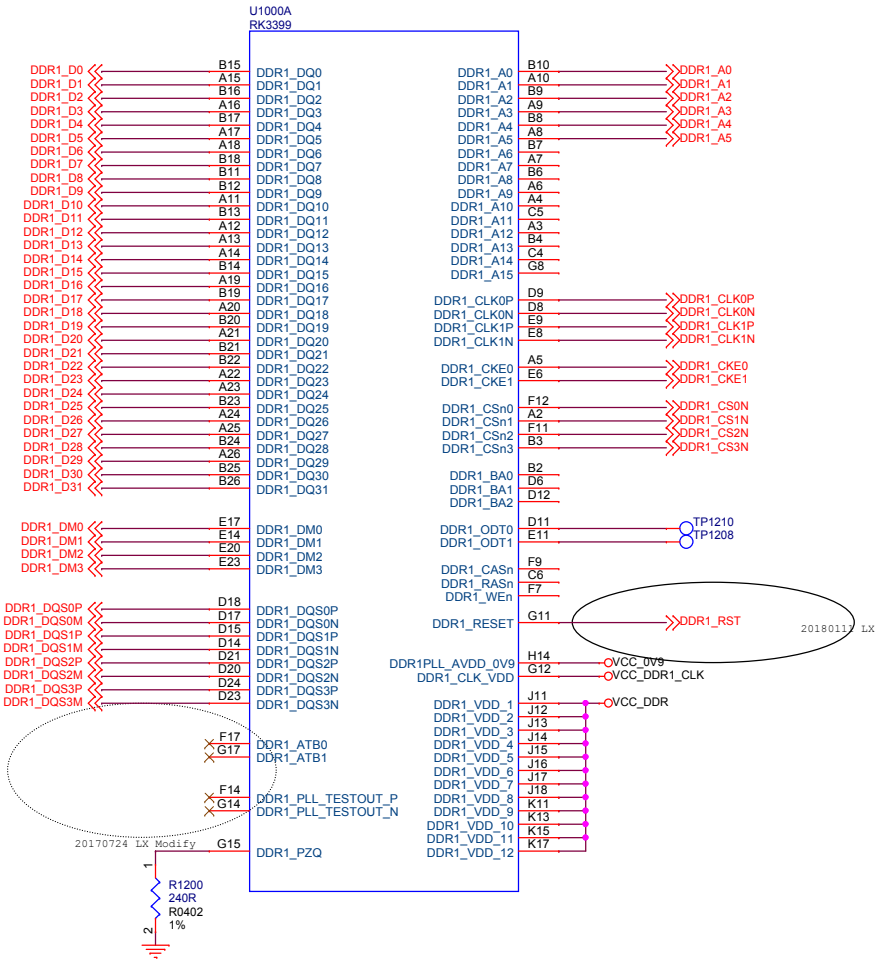

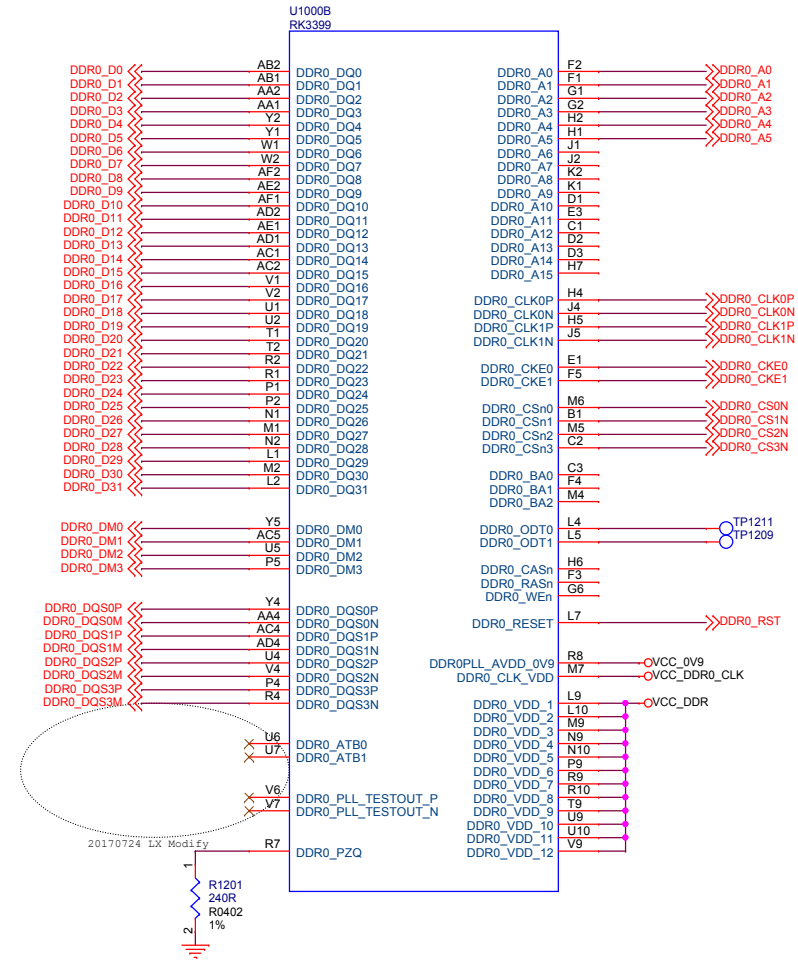

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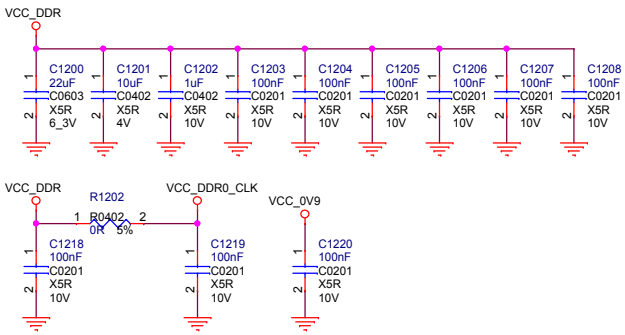

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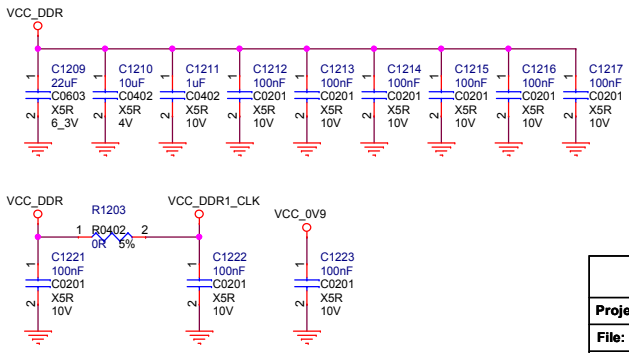

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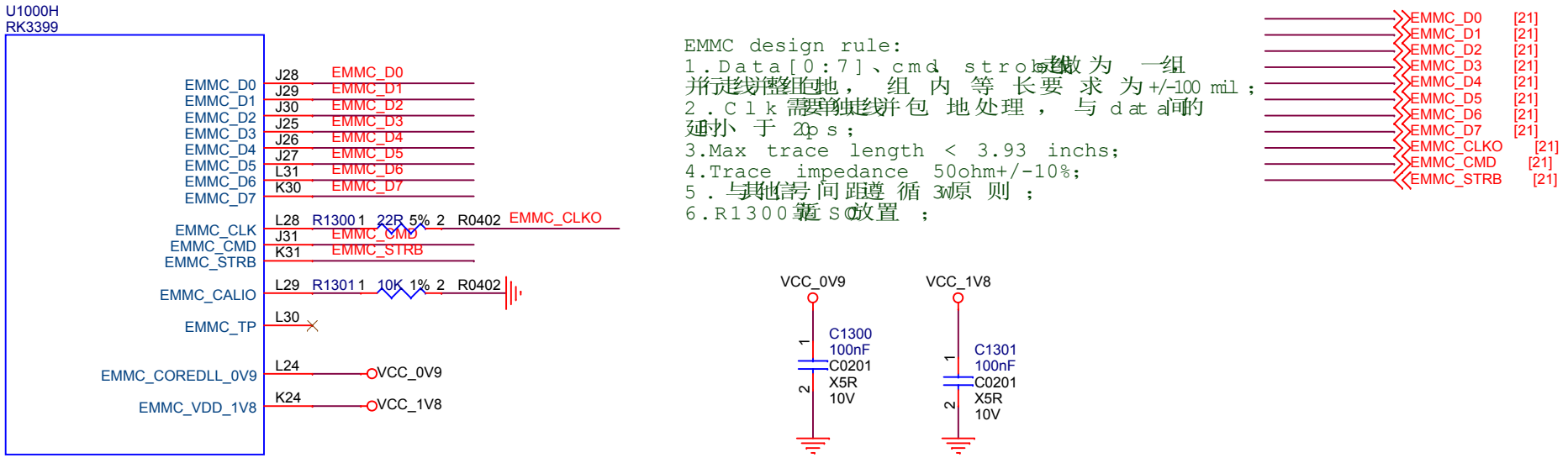

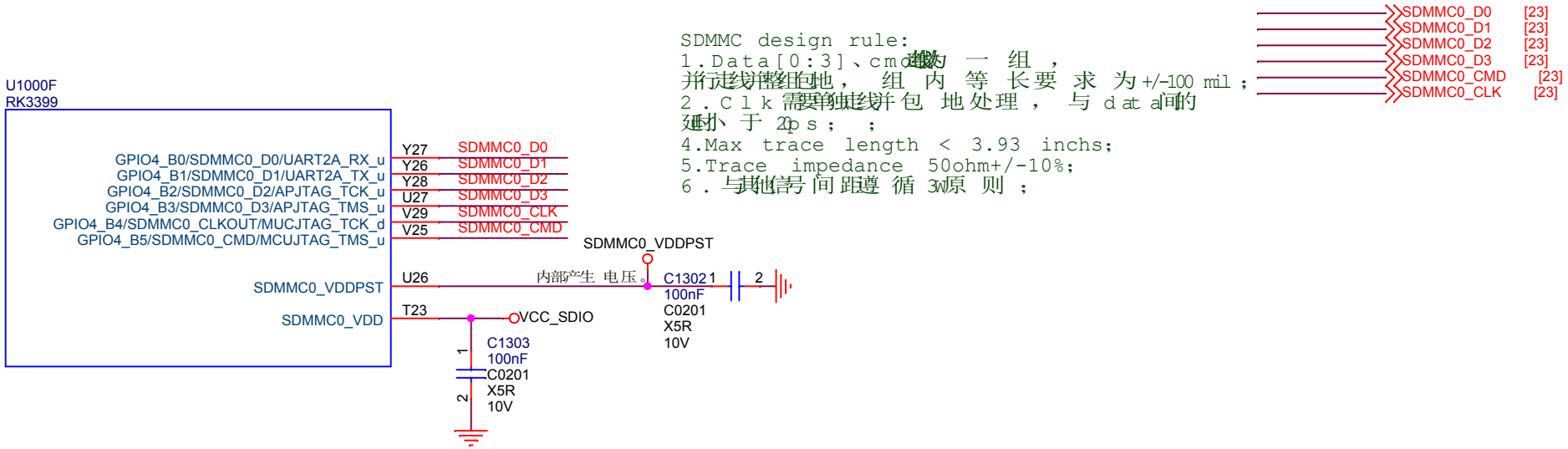

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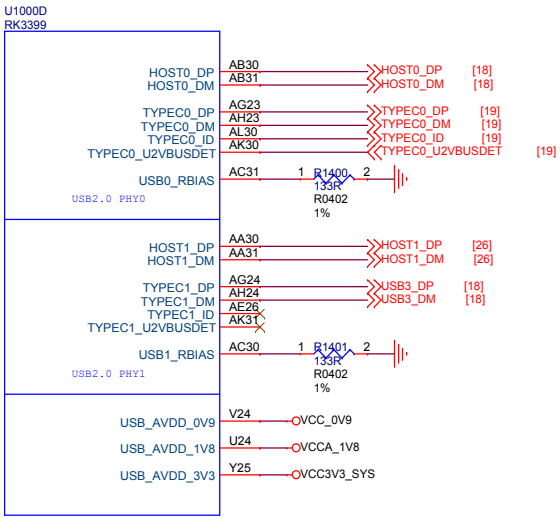
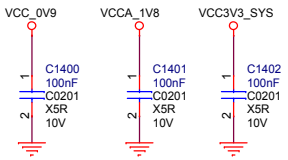
U1000U
RK3399

USIC_STROBE AJ30
USIC_DATA AJ31
USIC_AVDD_0V9 AD25
USIC_AVDD_1V2 AD24

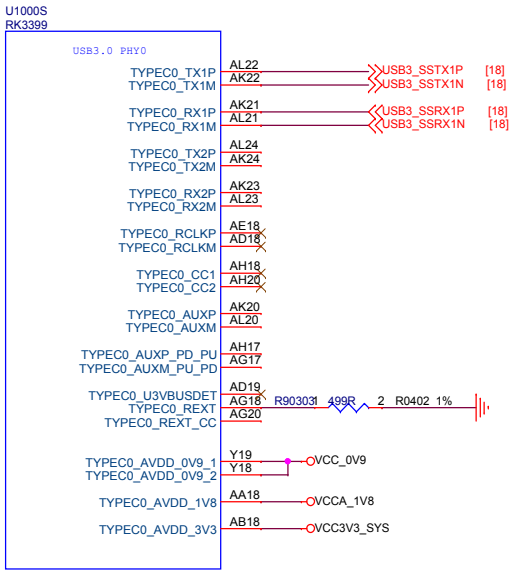
USB2.0

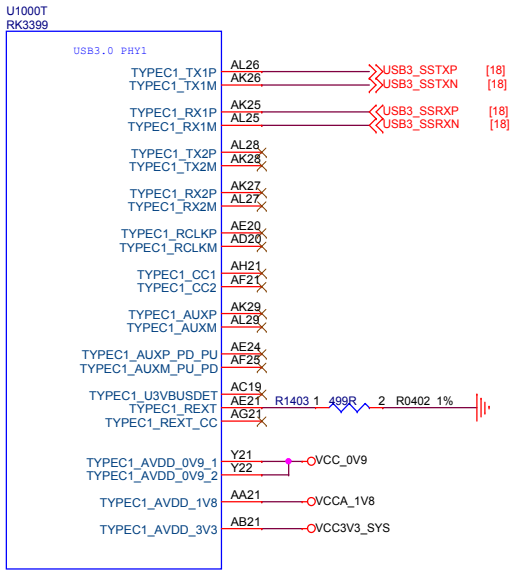


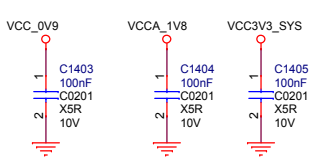


USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5．与其他信号间距遵循3W原则；

USB3.0







USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and RX < 1.6 ns;
3.Max trace length < 6 inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6．与其他信号间距遵循3W原则；

DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5．与其他信号间距遵循3W原则；

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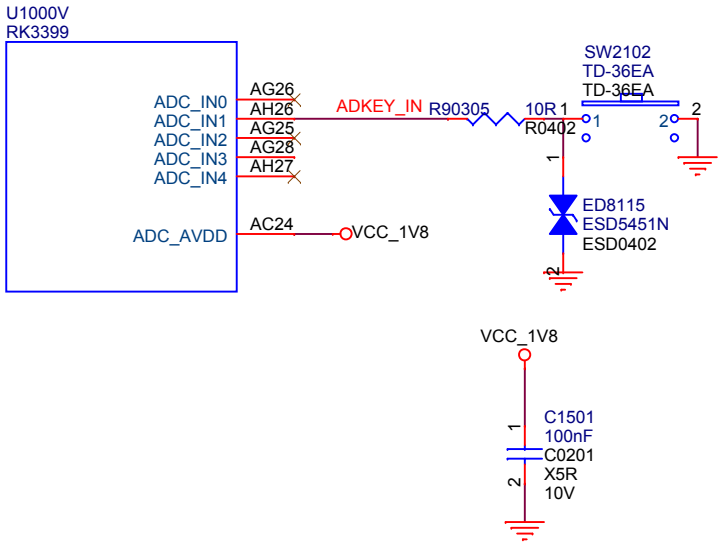
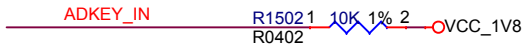


KEY BAORD

Note:
系统时，如果ADKEY_IN电平为0V，
则RK3399进入Recovery模式；
量产时R1503,SW1500,ED1500可以不用贴片;



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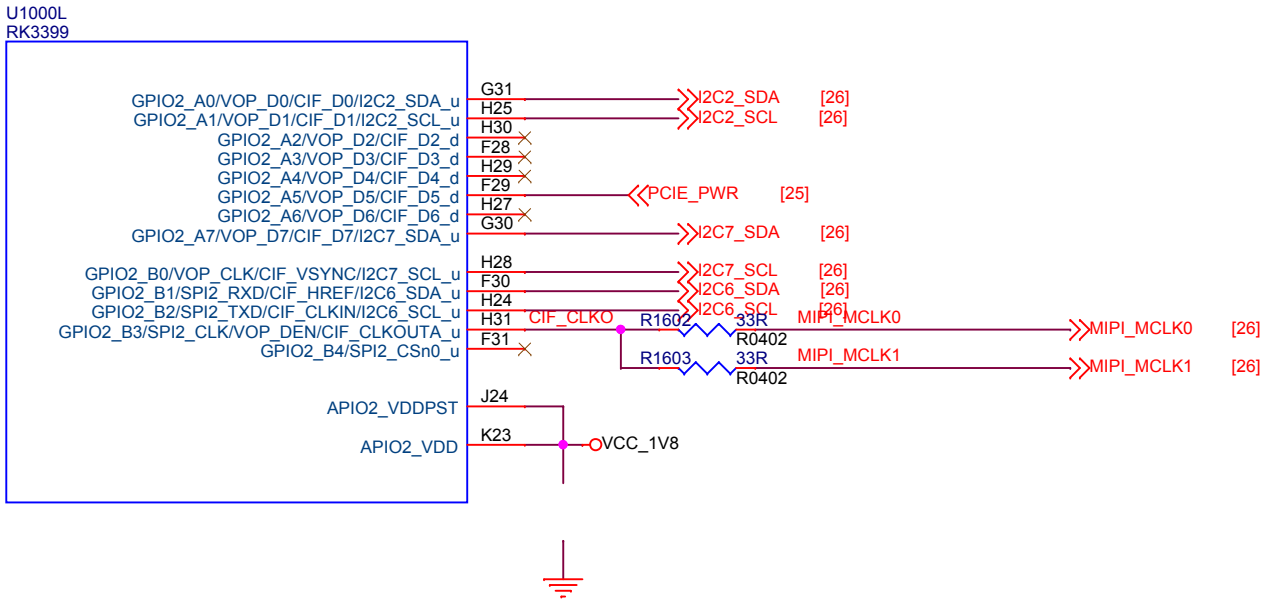

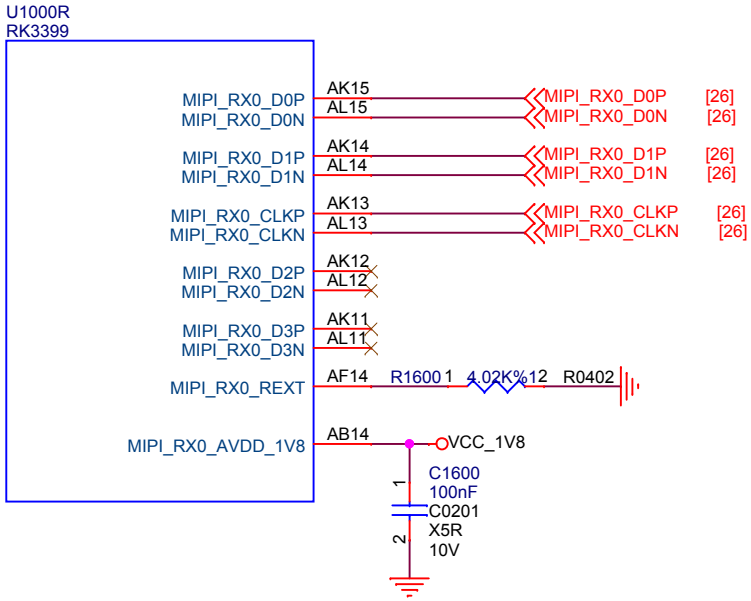

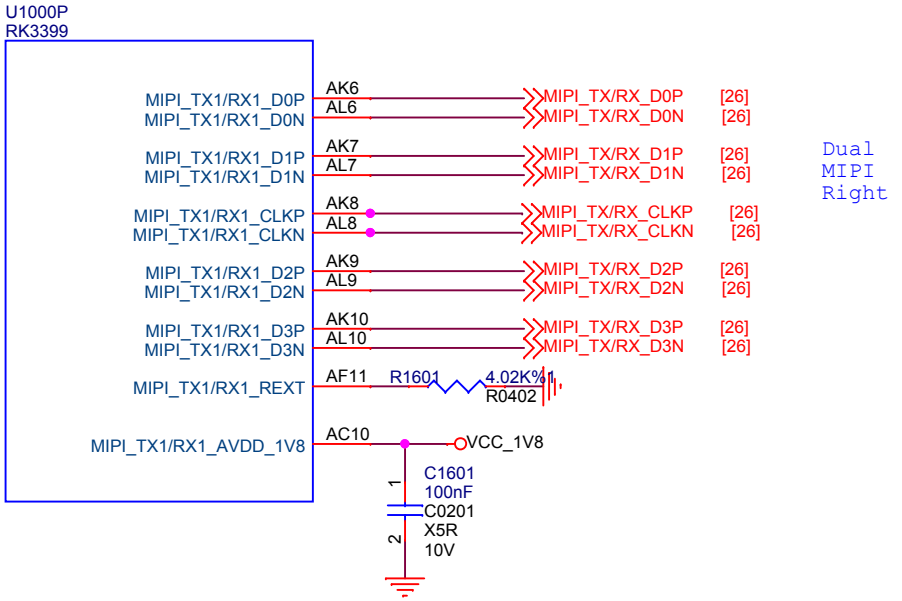

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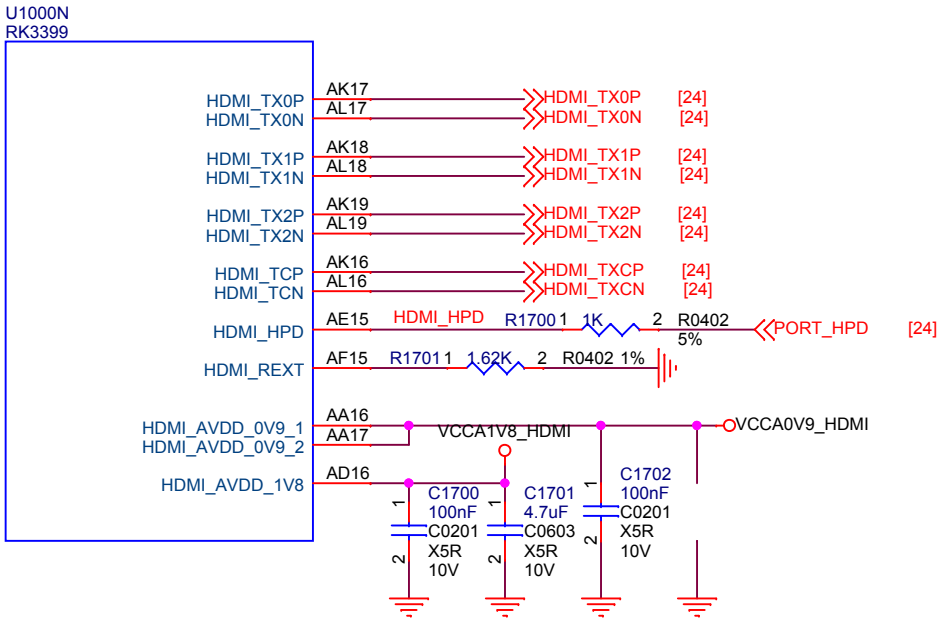
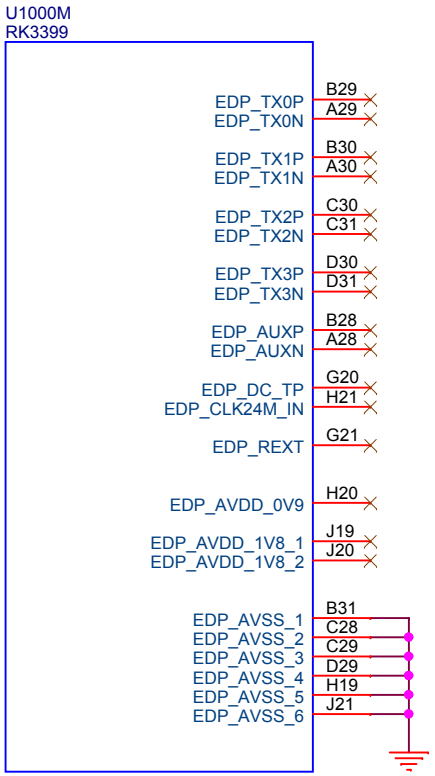
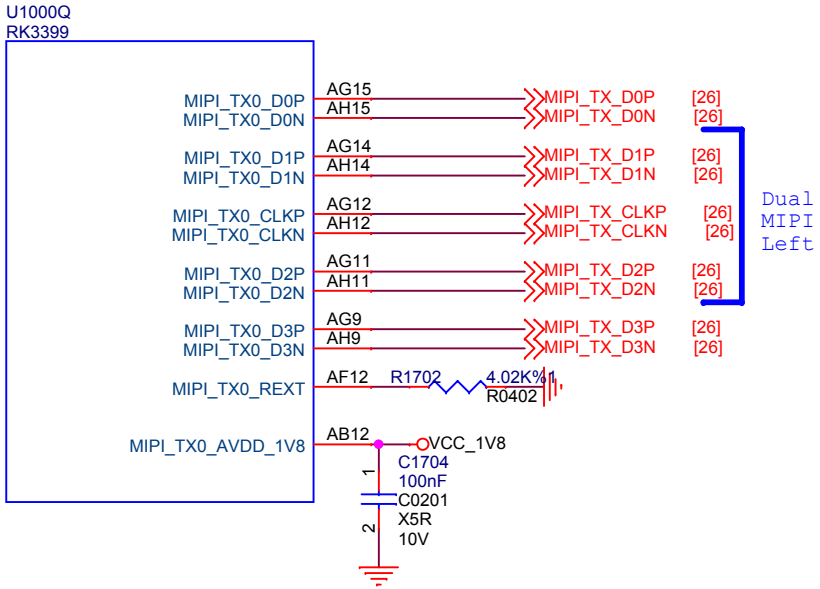


HDMI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 80 ps;
3.Max trace length < 9.8 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6 . 与其他信号 间 距遵 循 3W原 则 ;



eDP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5 . 与其他信号 间 距遵 循 3W原 则 ;



MIPI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6 . 与其他信号 间 距遵 循 3W原 则 ;

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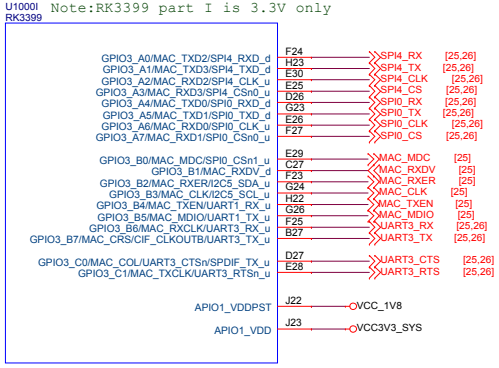
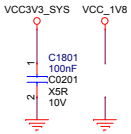
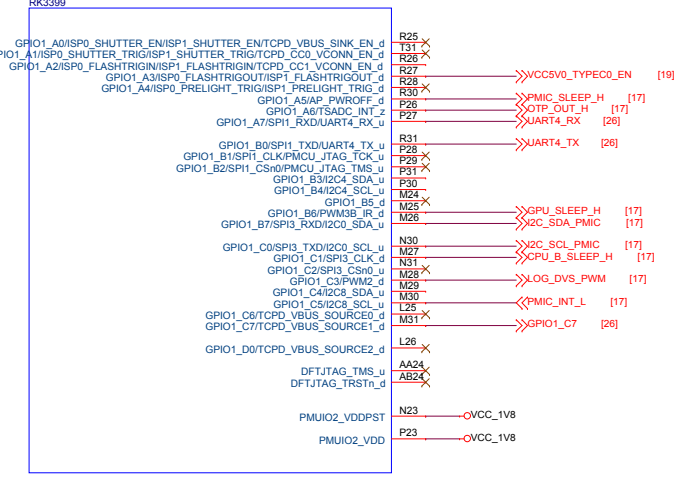
U1000I Note:RK3399 part I is 3.3V only
RK3399

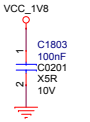


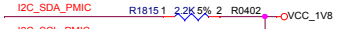


U1000E Note:RK3399 part E is 1.8V/3.0V mode
RK3399

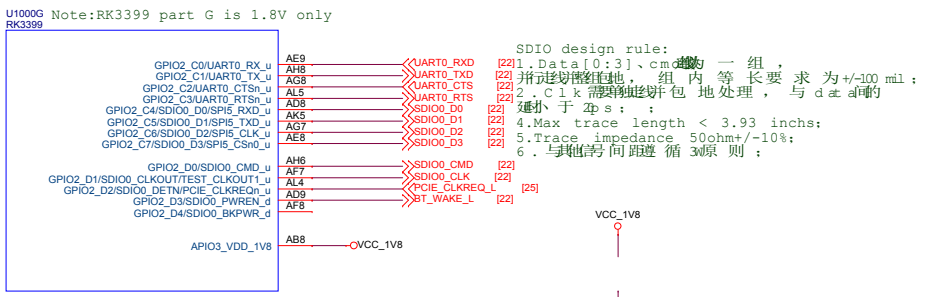


1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
other	3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V



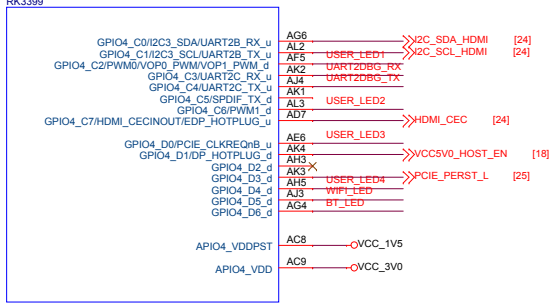


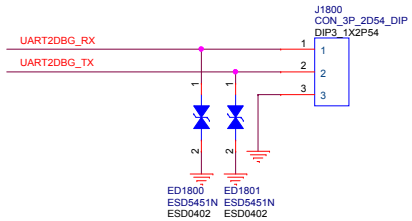
U1000G Note:RK3399 part G is 1.8V only
RK3399

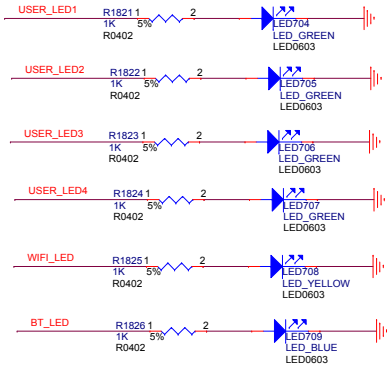


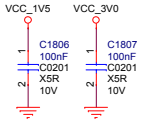
SDIO design rule:
1.Data[0:3]、cmd为一组，并走线时组内等长要求为+/-100 mil；
2.Clk需要独立包地处理，与data的间距大于2倍；
3.Trace impedance 50ohm+/-10%;
4.Max trace length < 3.93 inchs;
5.Trace impedance 50ohm+/-10%;
6.与其他信号间距遵循3W原则；

U1000K Note:RK3399 part J is 1.8V/3.0V mode
RK3399

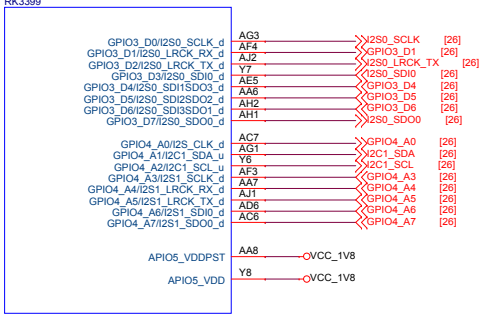


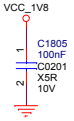






U1000J Note:RK3399 part J is 1.8V/3.0V mode
RK3399





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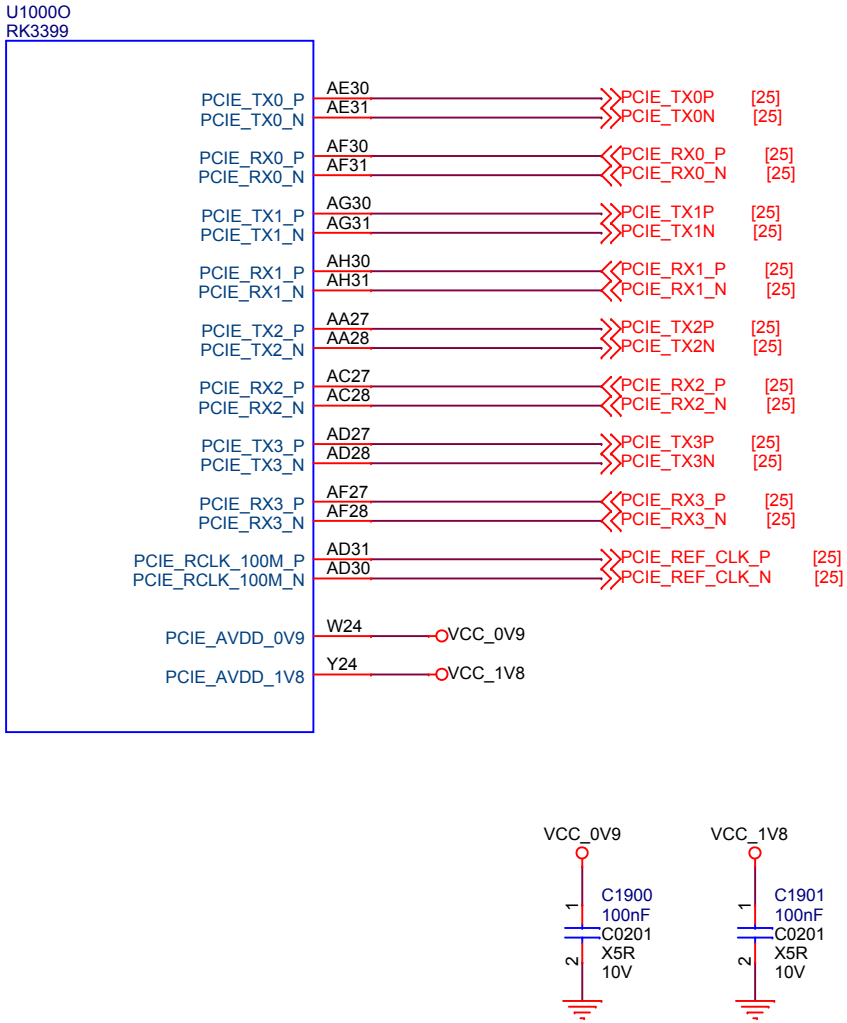

PCIE design rule:
1.Max intra-pair skew < 4ps;
2.Max inter-pair skew < 1.6 ns;
3.Max trace length < 14 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6 . 与其他信号 间距遵 循 3W原 则 ;

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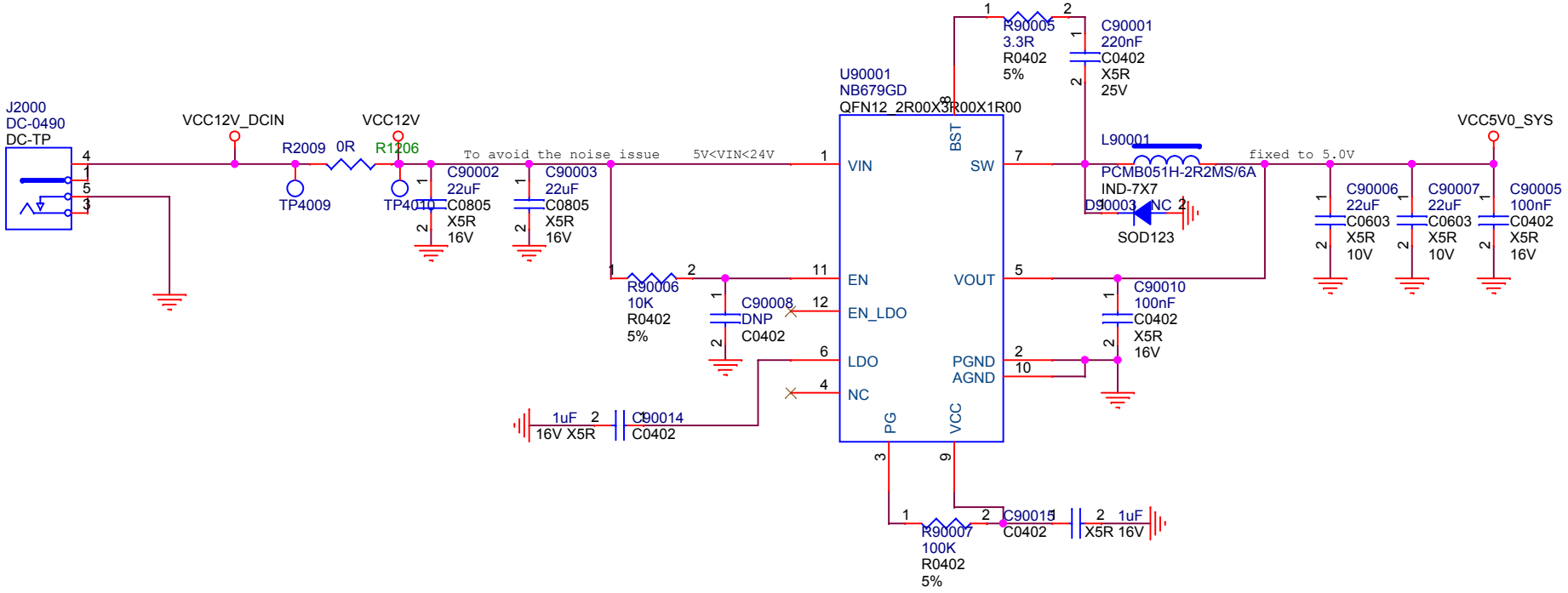
DC IN&SYSTEM Power



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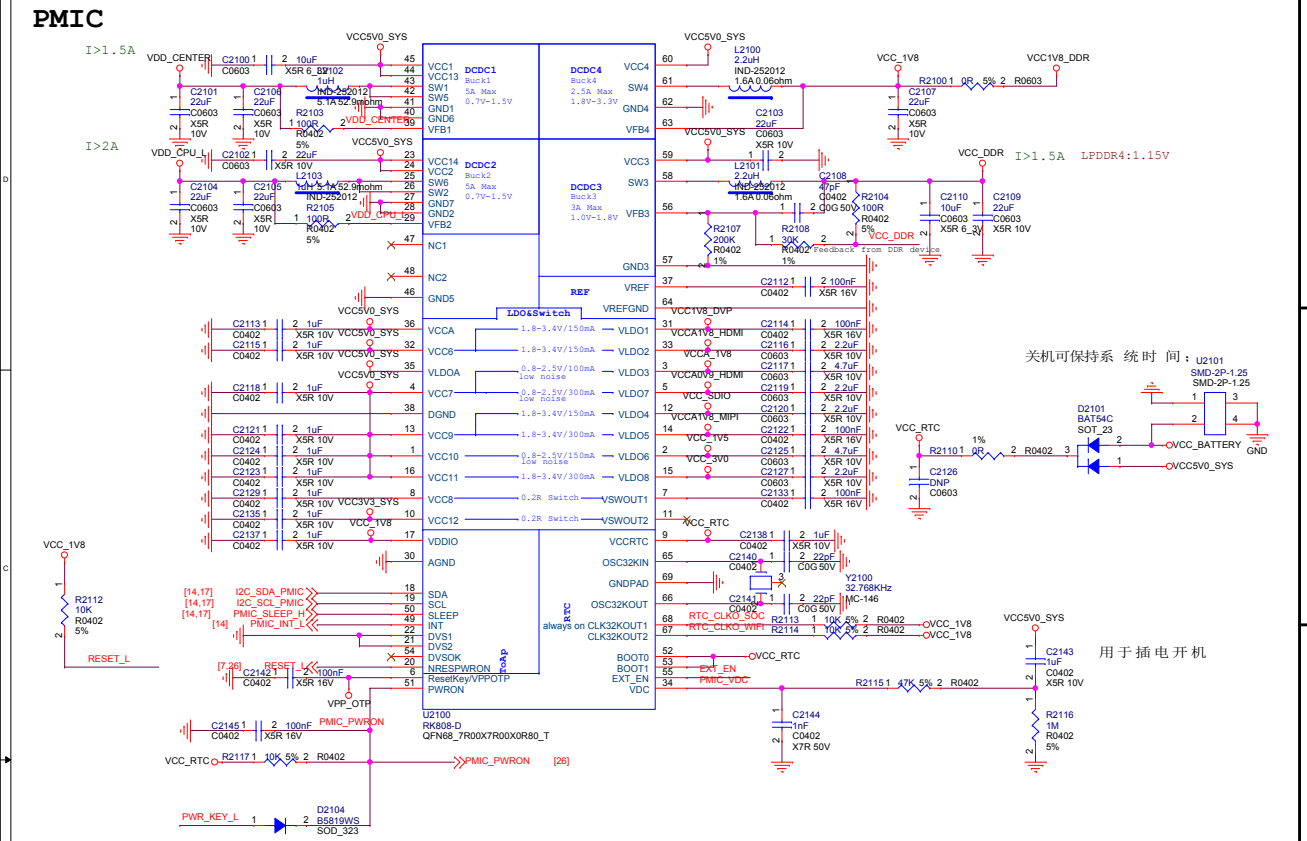
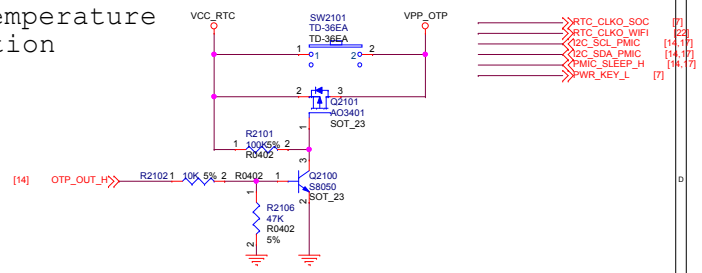
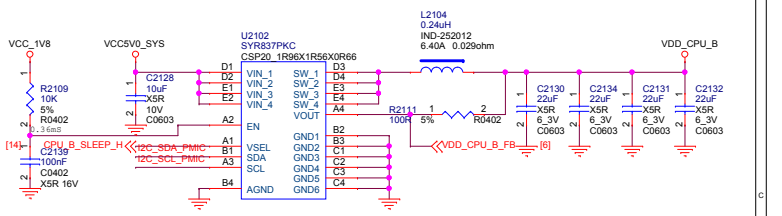
PMIC



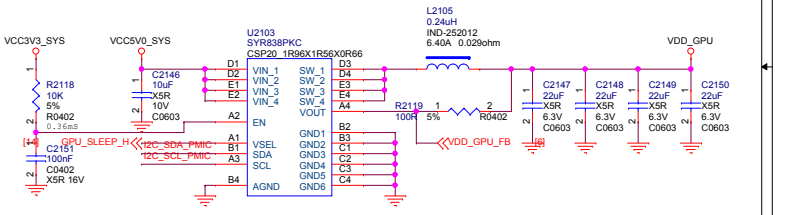
Over-temperature Protection



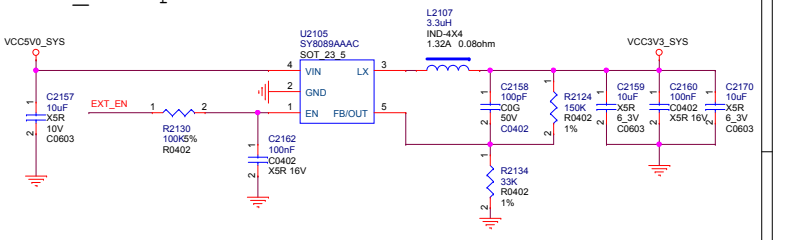
VDD_CPU_B power



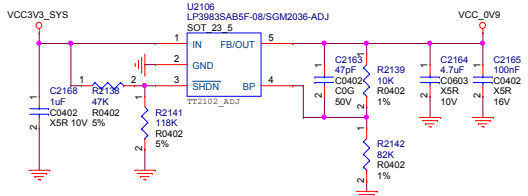
VDD_GPU power



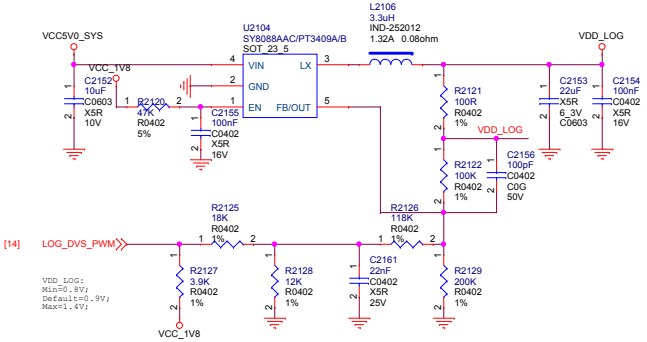
VCC3V3_SYS power



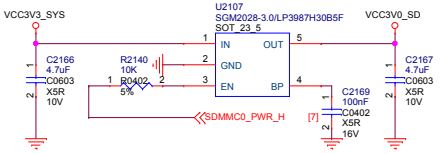
VCC_0V9 power



VDD_LOG power



VCC3V0_SD power



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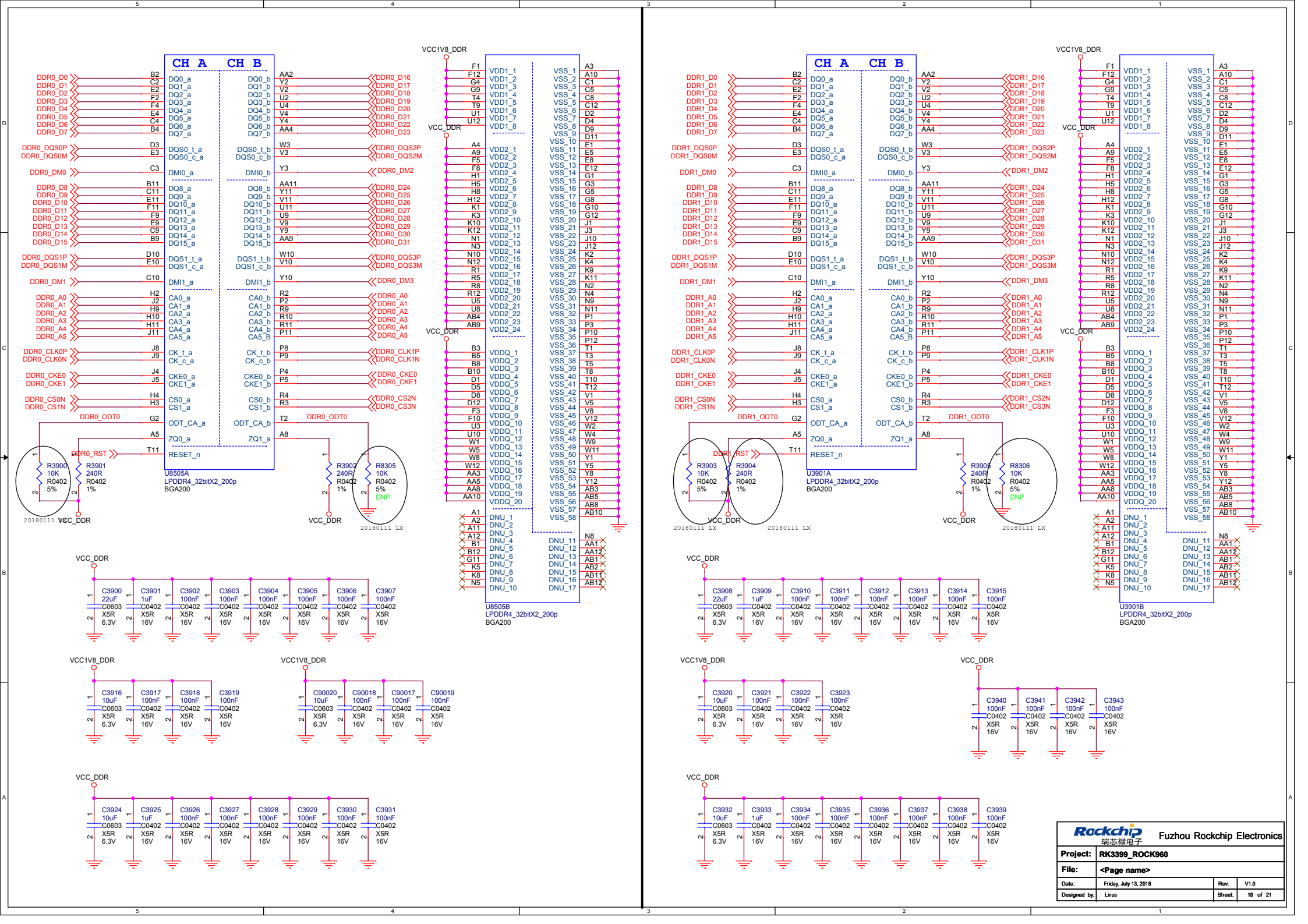
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CH B
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BGA200
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LPDDR4_32bitX2_200p
BGA200
U3901B
LPDDR4_32bitX2_200p
BGA200
VCC1V8_DDR
VCC_DDR
DDR0_ODT0
DDR0_RST
DDR1_ODT0
DDR1_RST
R3900 10K R0402 5%
R3901 240R R0402 1%
R3902 240R R0402 1%
R8305 10K R0402 5% DNP
R3903 10K R0402 5%
R3904 240R R0402 1%
R3905 240R R0402 1%
R8306 10K R0402 5% DNP
20180111 LX
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
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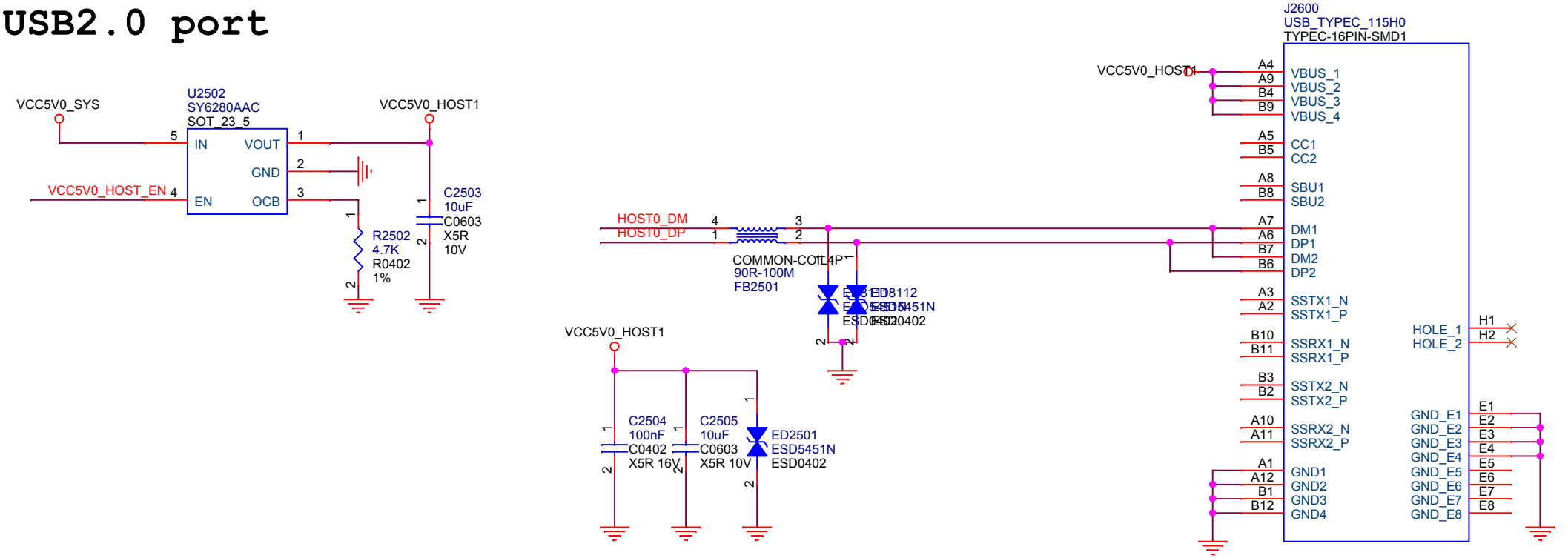
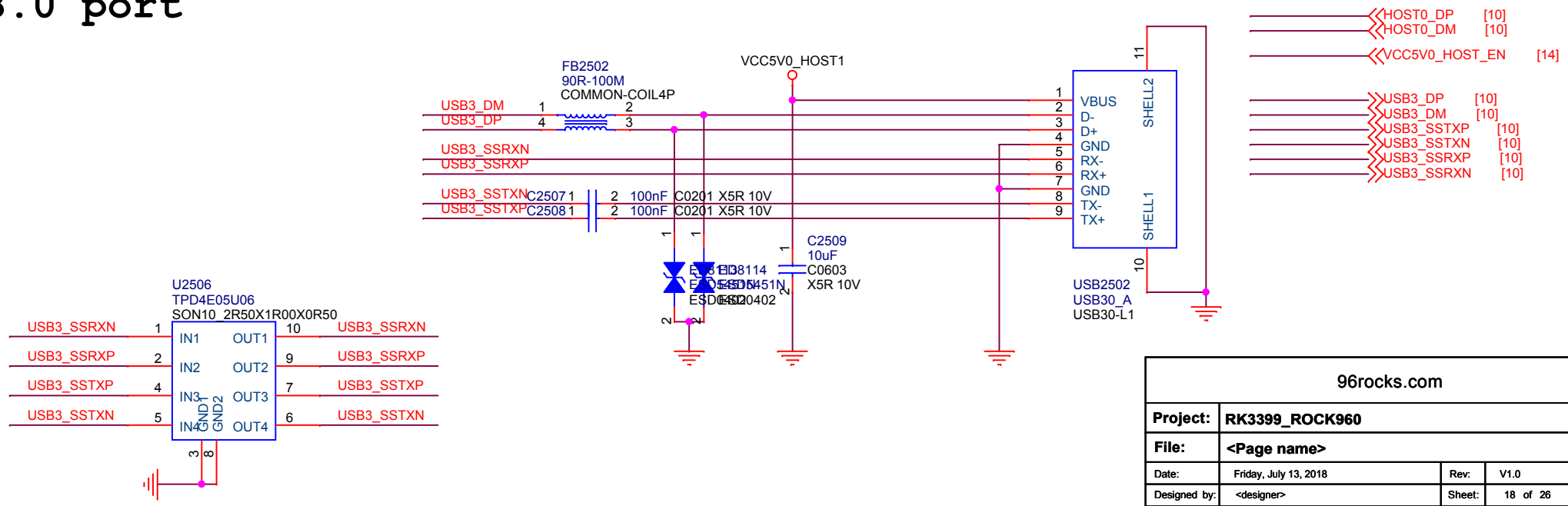
USB2.0 port



USB3.0 port



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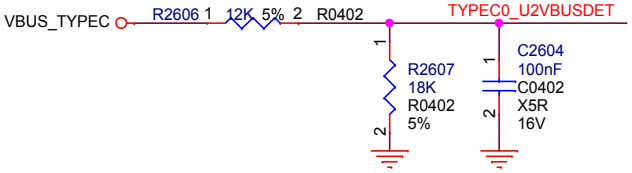
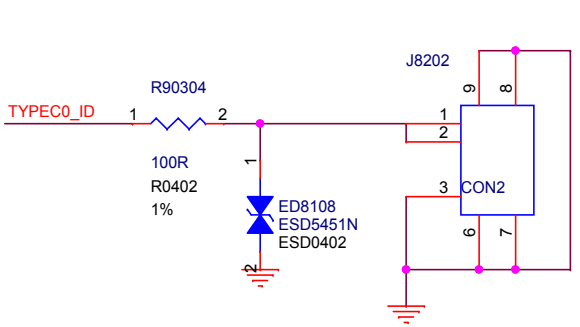
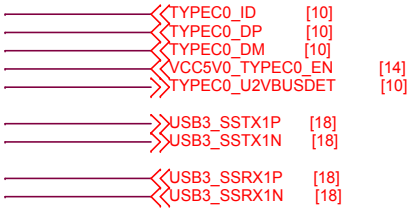
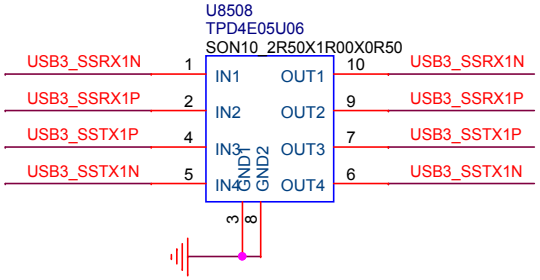
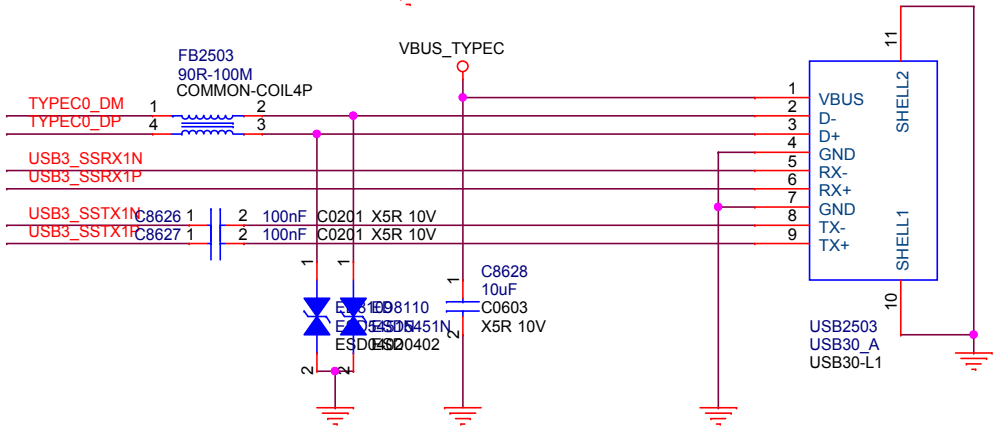
USB3.0 OTG port

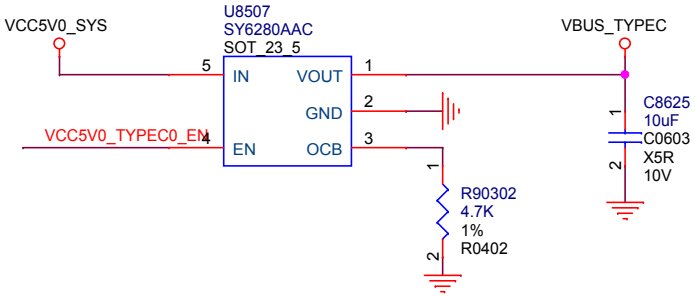












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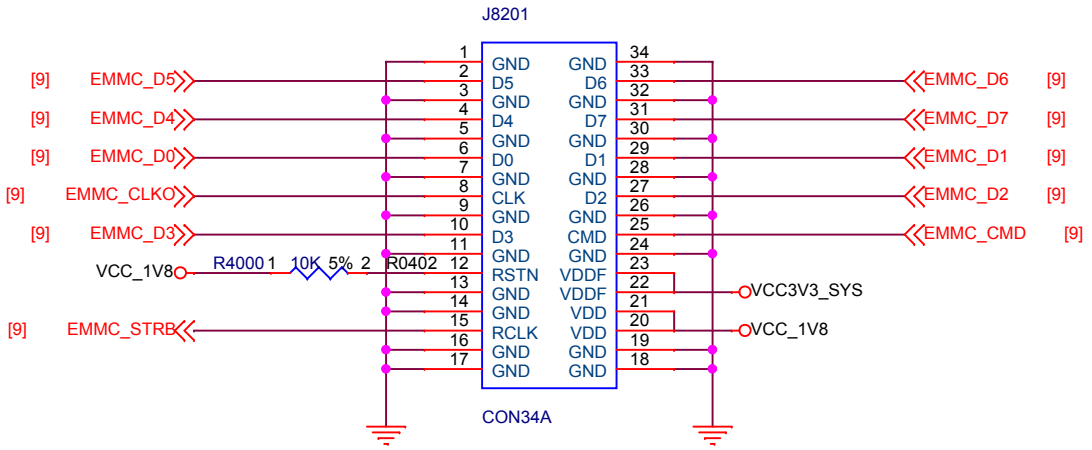
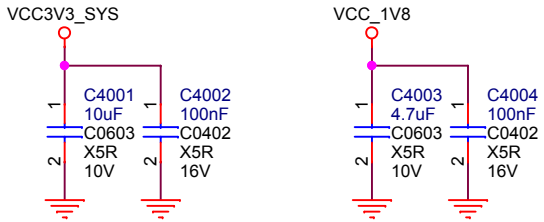
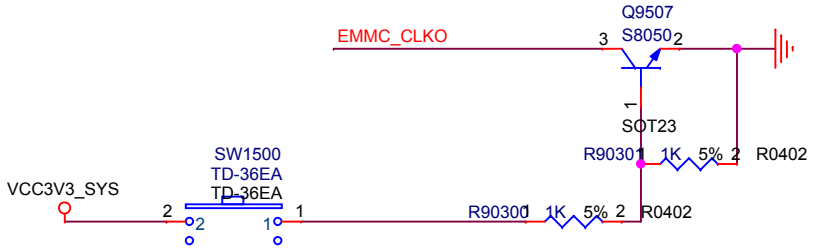
eMMC FLASH







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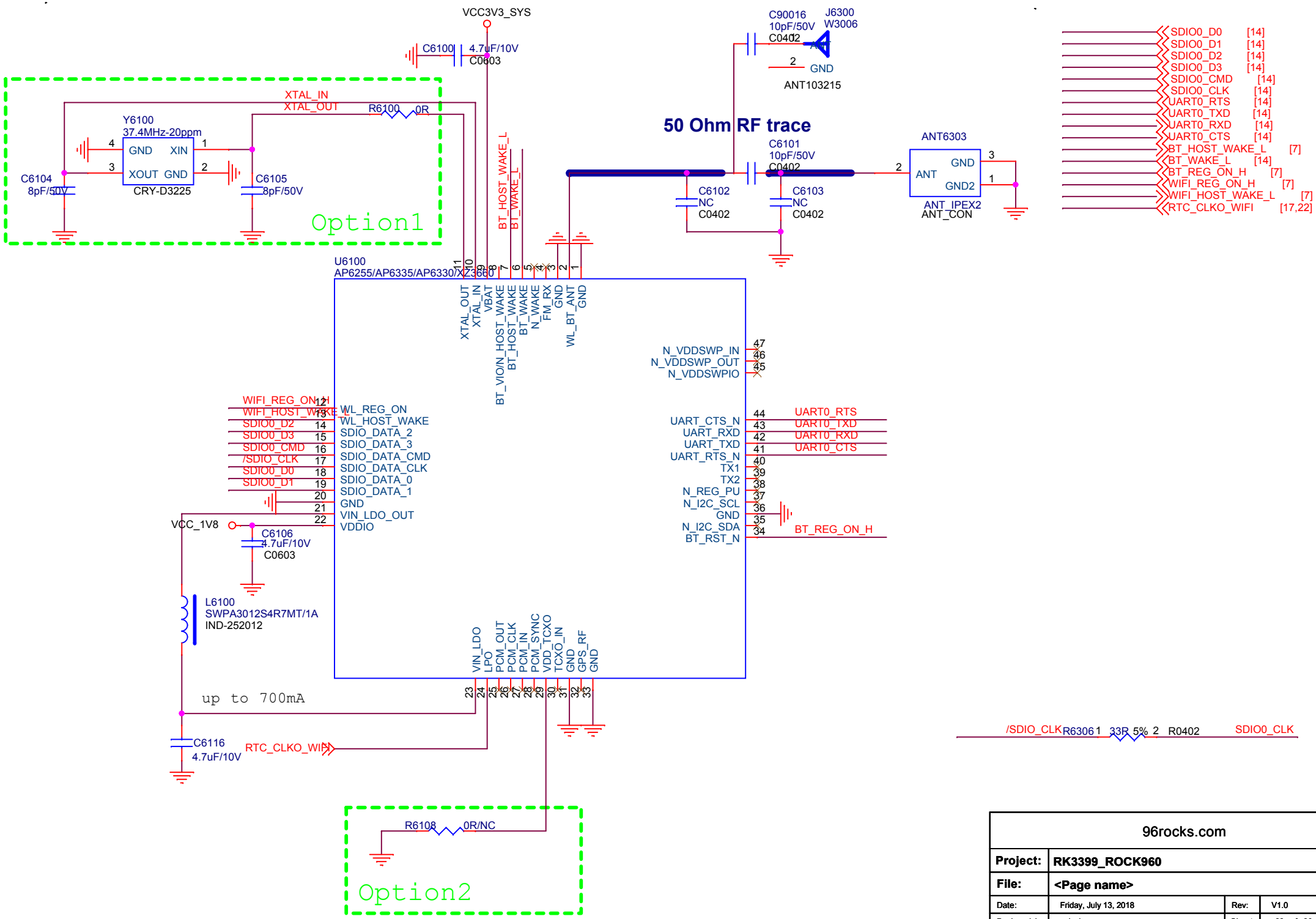

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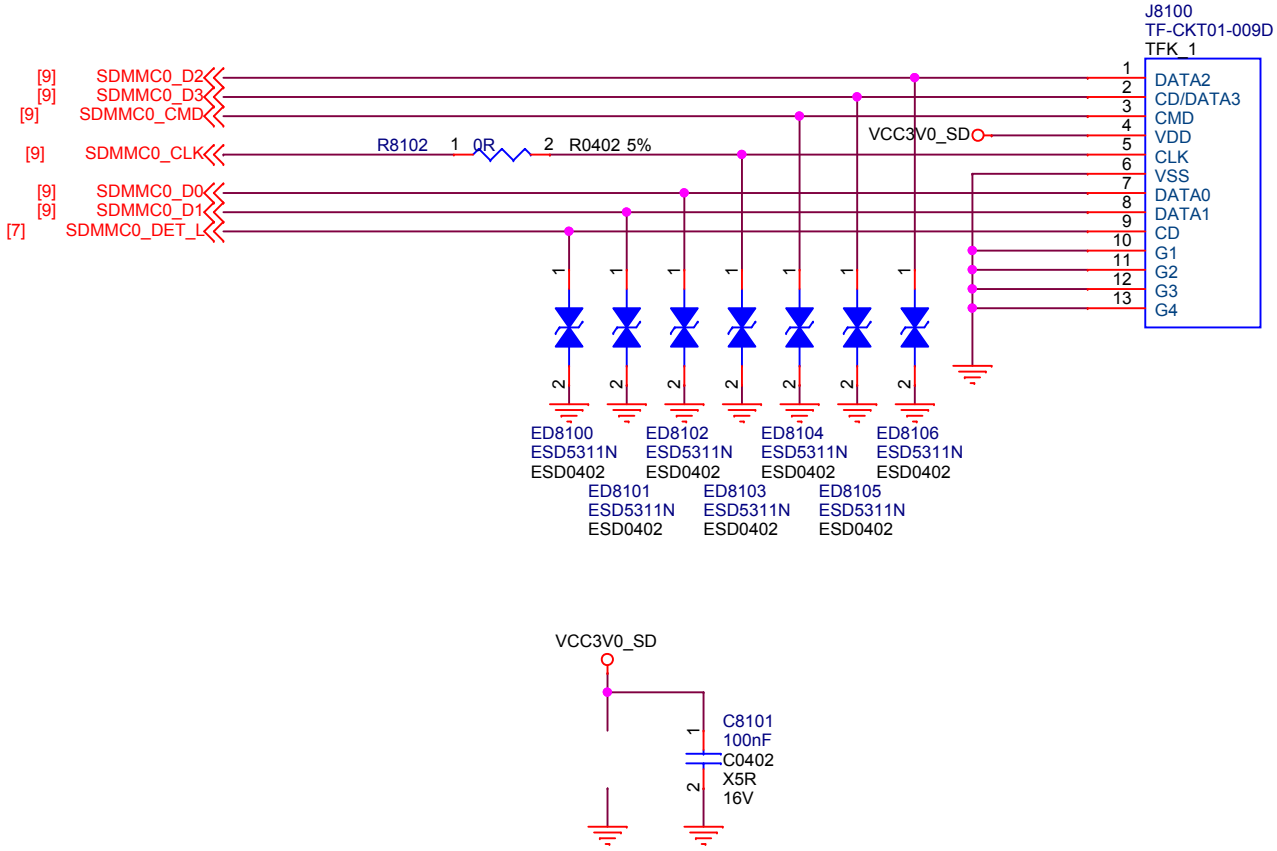
TF CARD



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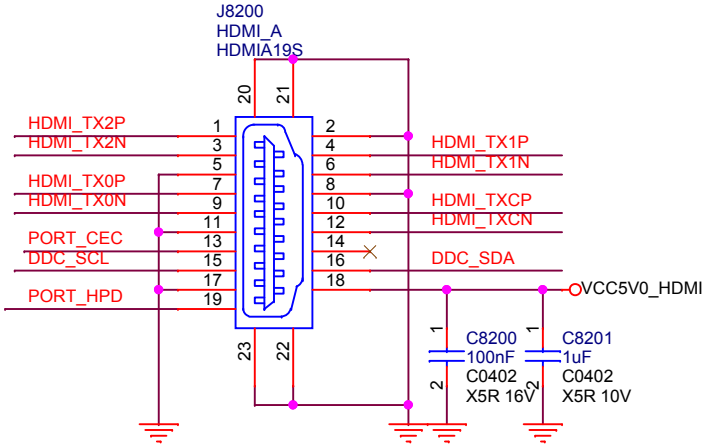
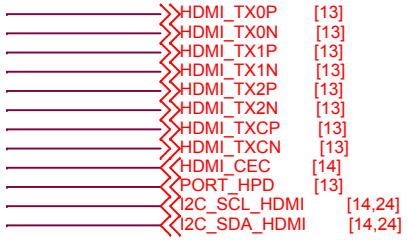
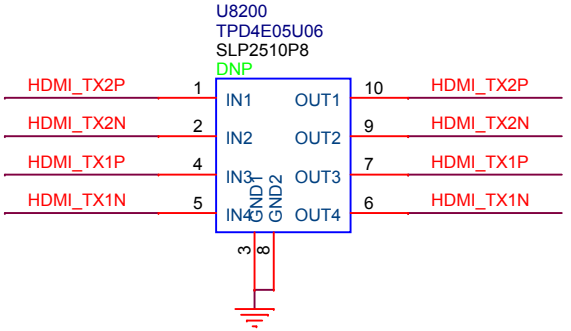
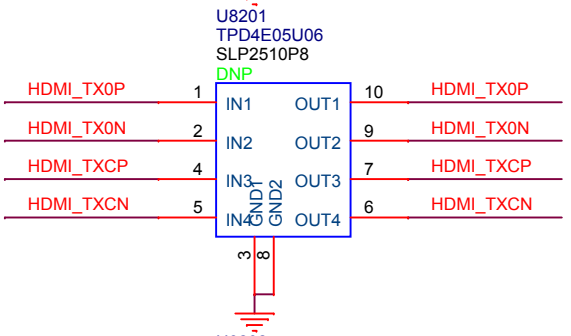
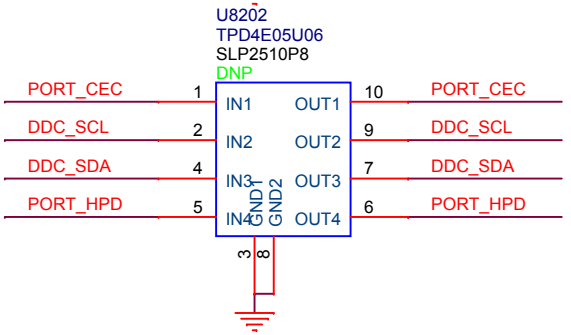
HDMI Output

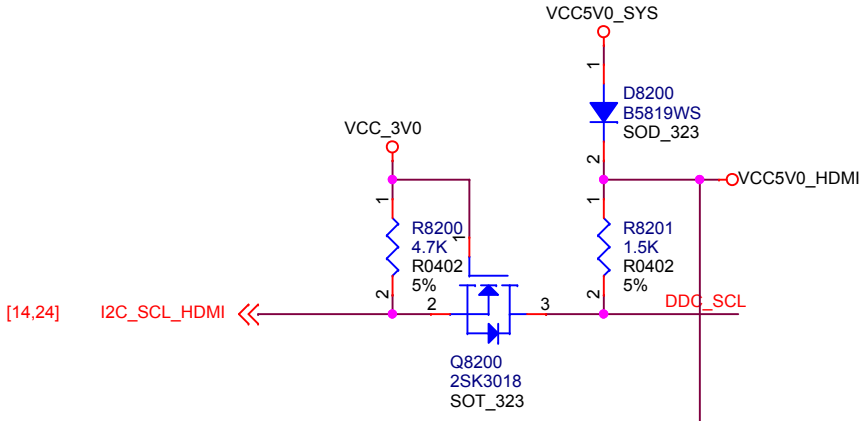


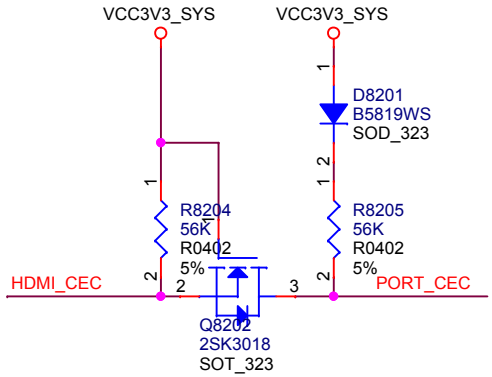












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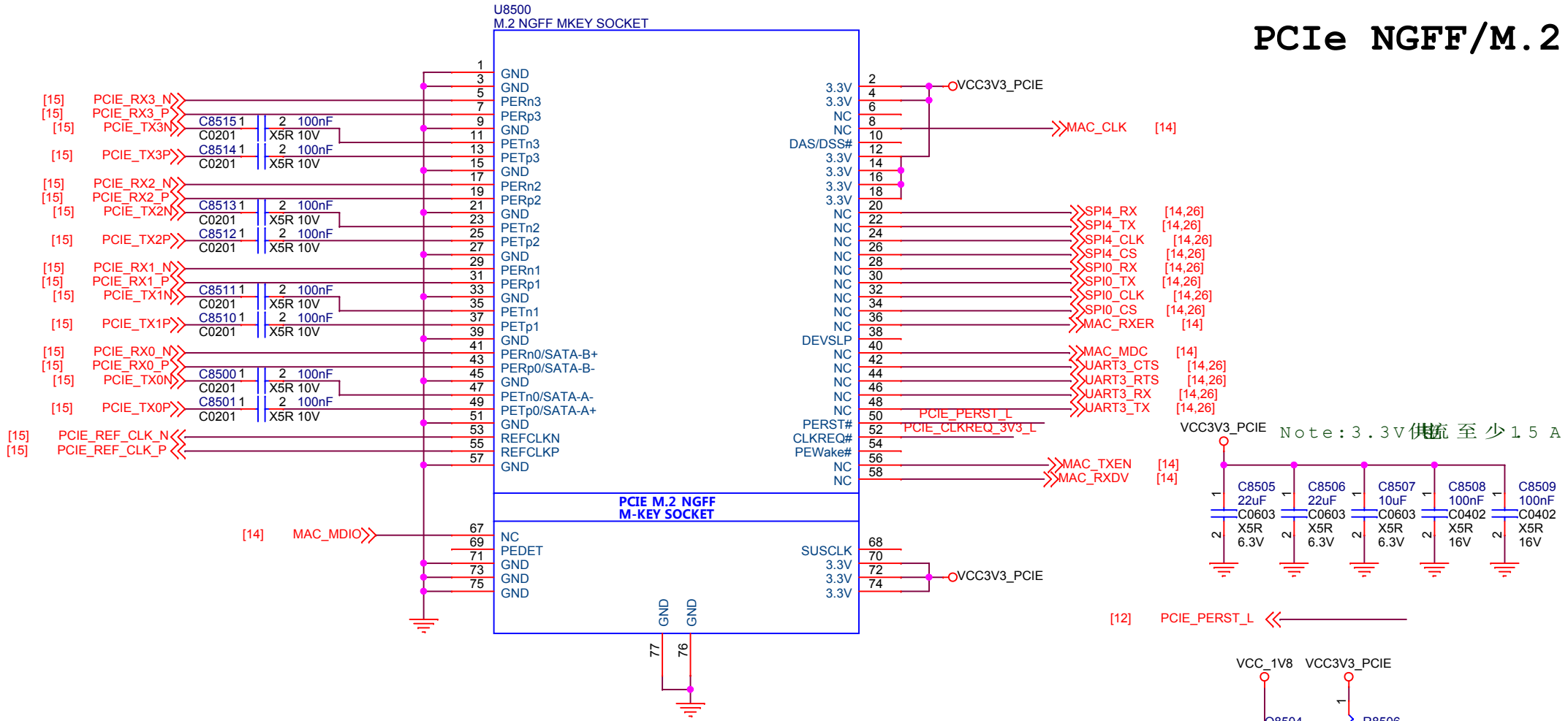
PCIe NGFF/M.2



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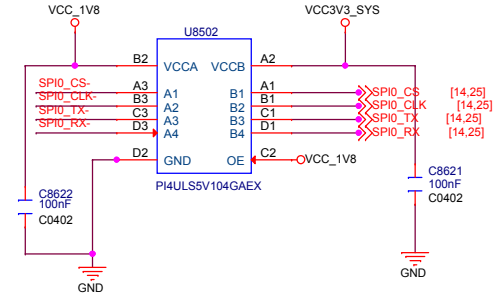
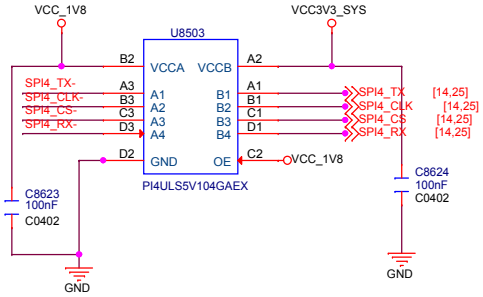
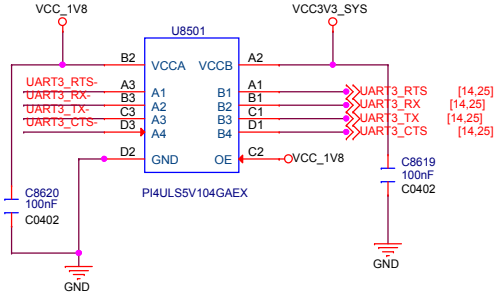
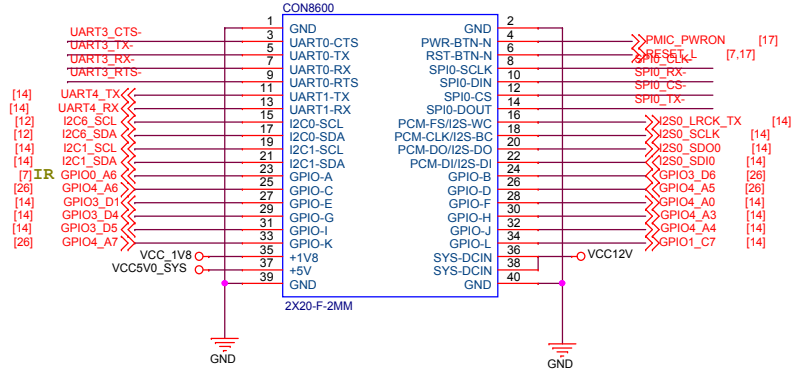
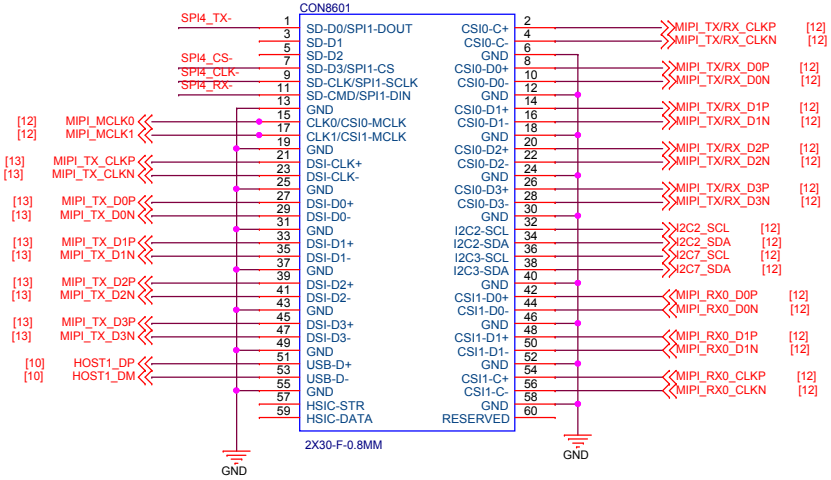
注意：
電壓VCCB>=VCCA。











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