

RK3399_Rock960_V1.2

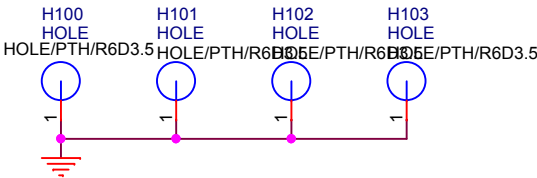
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6 LAYERS PCB STACK é g PCB=1.6mm

TOP		Silkscreen 0.25mm 1oz (35um)
	Prepreg 1080*1 (75um)	
GND1		Hoz (18um)
	Prepreg 2116*1 (115um)	
POWER		Hoz (18um)
	Adjust Core 0.65mm	
SIGNAL		Hoz (18um)
	Prepreg 2116*1 (115um)	
GND2		Hoz (18um)
	Prepreg 1080*1 (75um)	
BOTTOM		1oz (35um) Silkscreen 0.25mm

Note:
器件参数说明
1:如果 Value 为 DP,说明暂时不贴。
2:如果 Option 有 DP,说明预留先不贴。

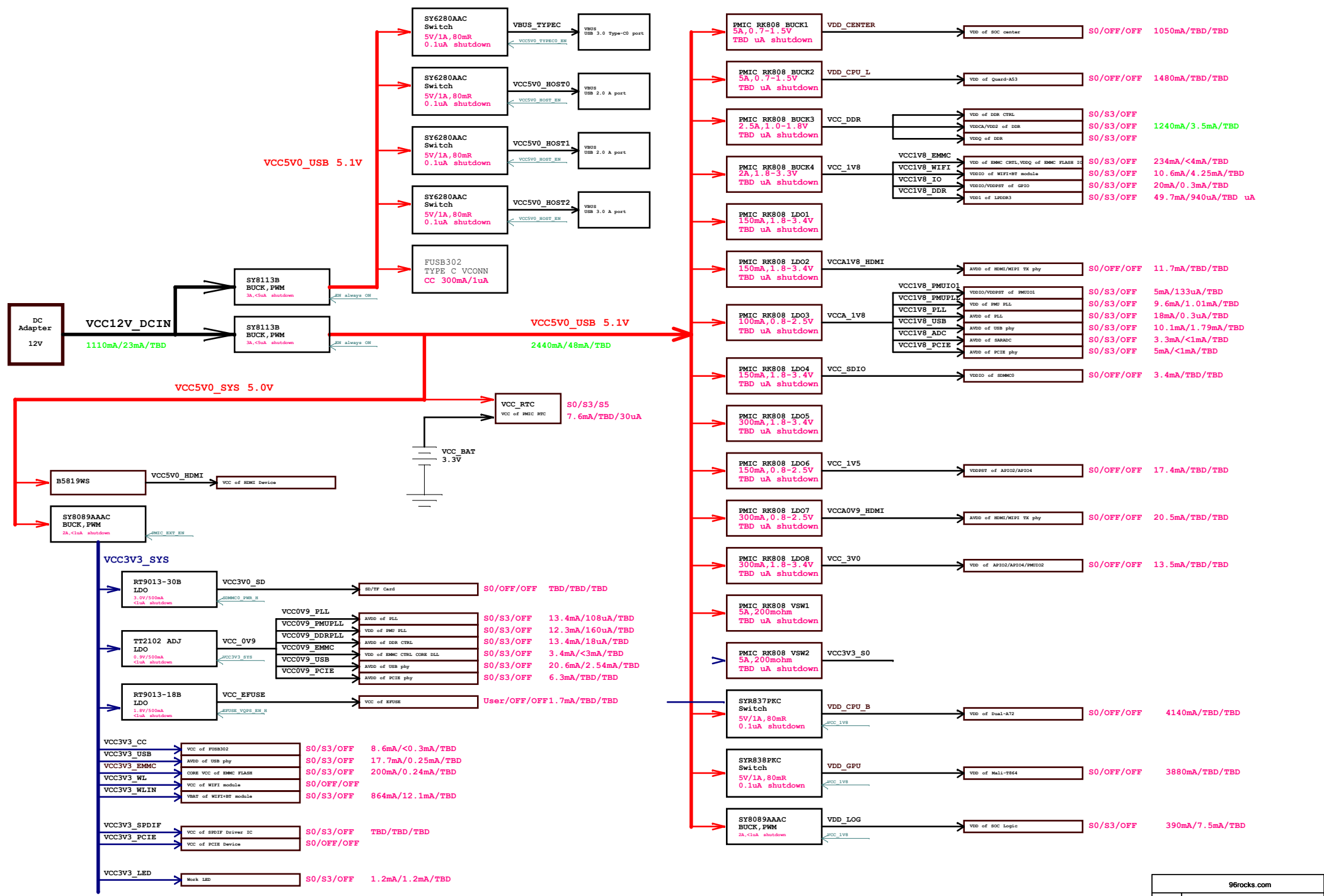


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Change List

Version	Date	Author	Change Note	Approved
V1.0	201708	Charlie	First edition	

RK3399 POWER DIAGRAM

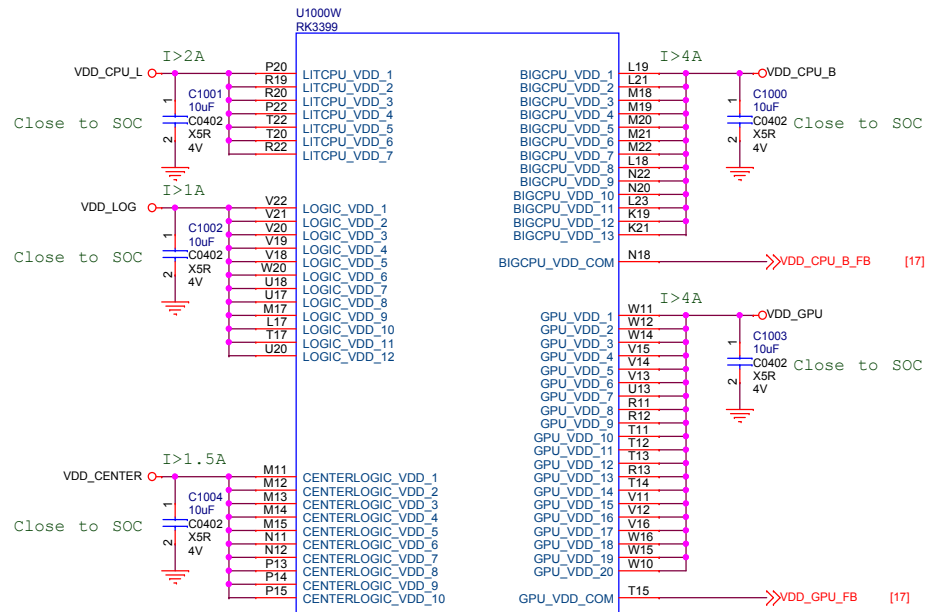


I2C MAP

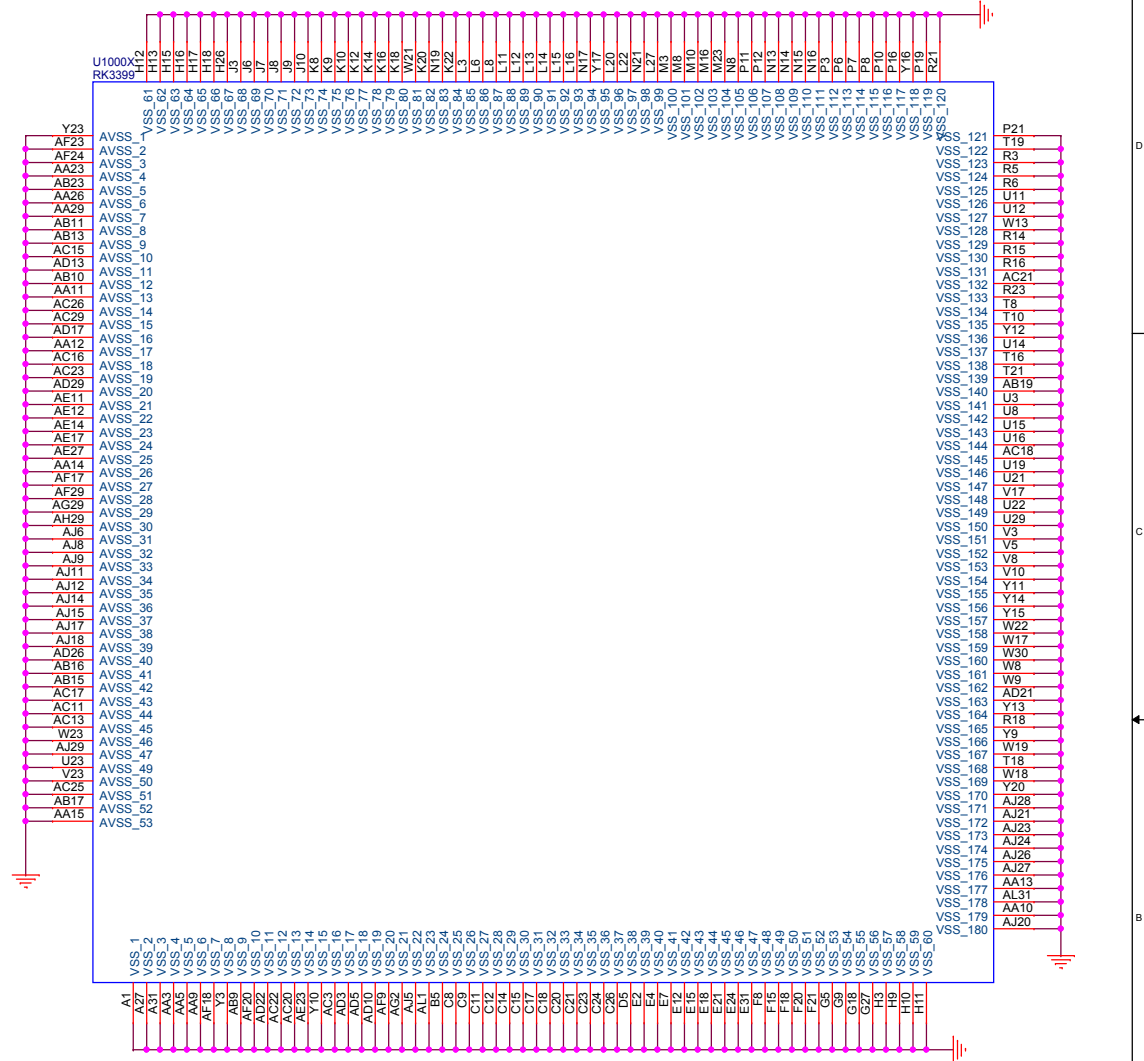
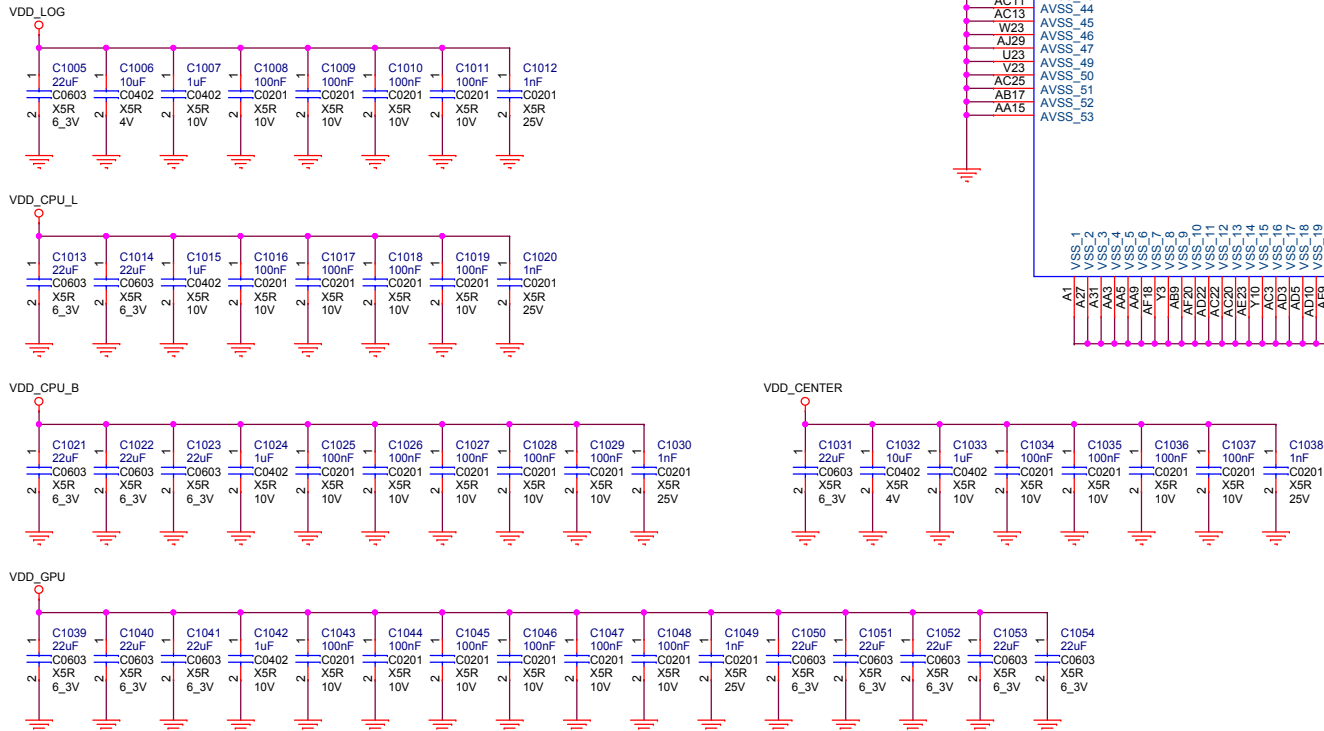
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5		VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECTOR	
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	

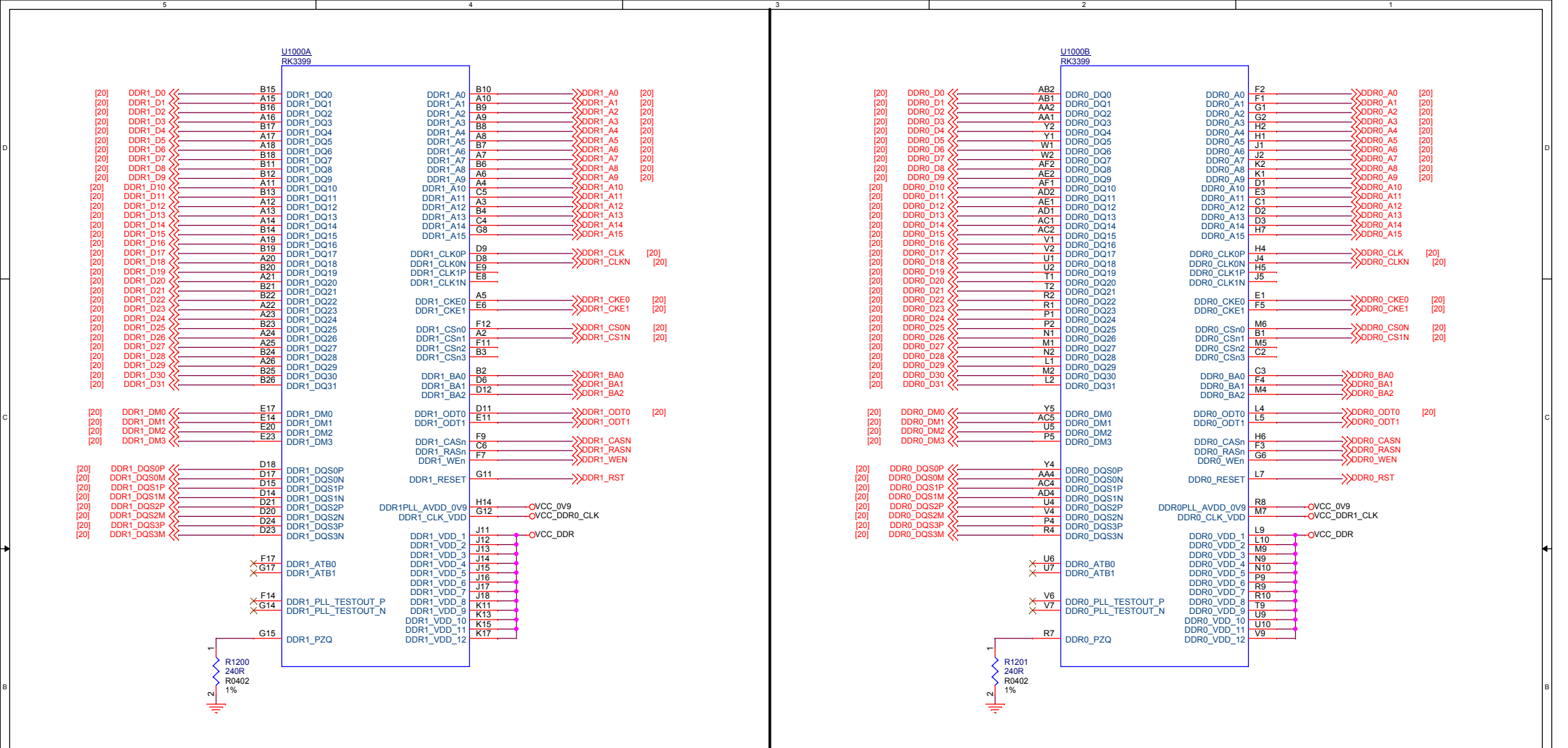
Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuiol_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmul830_gpio1abcd	1.8V (Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_SYS	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V (Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V (Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V (Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V (Default)	VCC_SDIO	RK808-D VLDO4



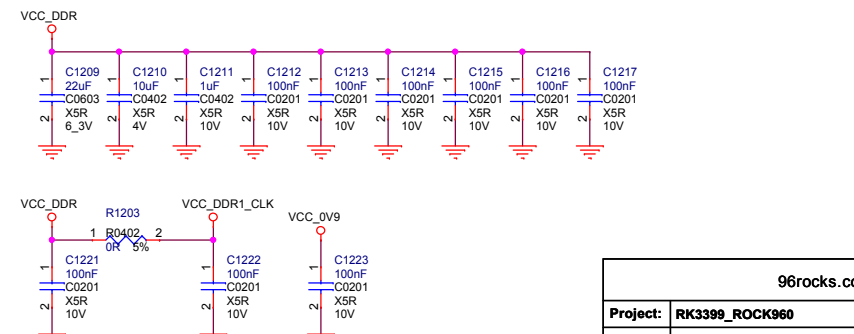
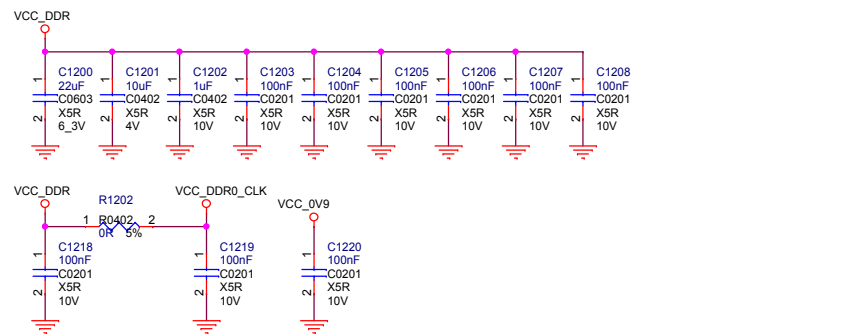
Note: Power filter CAP please place back of SOC or close to SOC



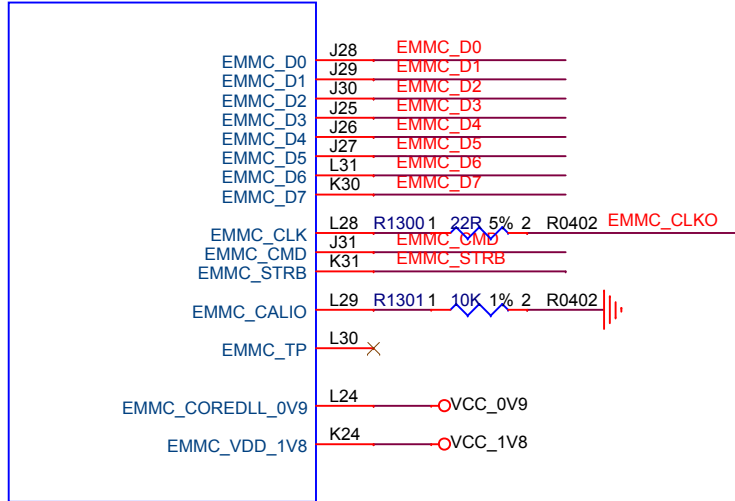


DDR FILTER Note:R1202 cannot be deleted

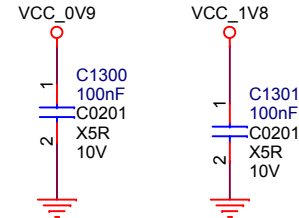
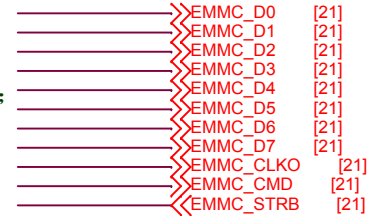
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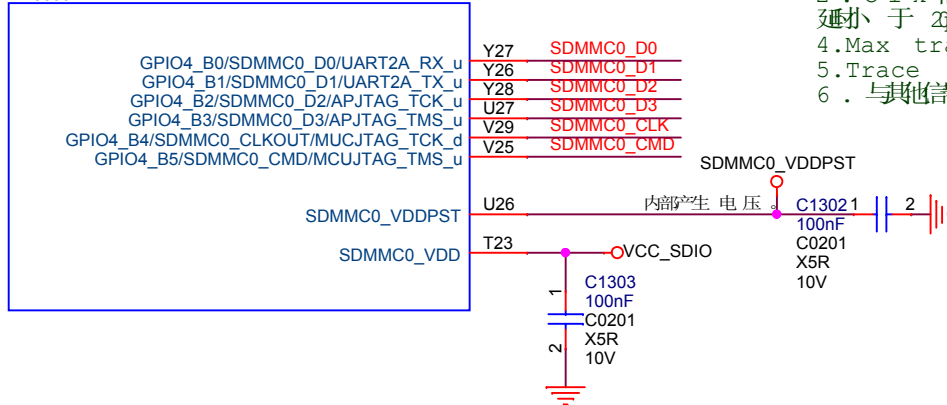
U1000H
RK3399



EMMC design rule:
1. Data[0:7]、cmd strobe 线做为一组
并行走线并包地，组内等长要求为+/-100 mil；
2. Clk 需要独走线并包地处理，与data间的
延时小于 2ps；
3. Max trace length < 3.93 inches；
4. Trace impedance 50ohm+/-10%；
5. 与其他信号间距遵循 3W 原则；
6. R1300 靠 SOC 放置；



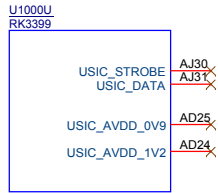
U1000F
RK3399



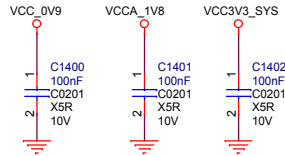
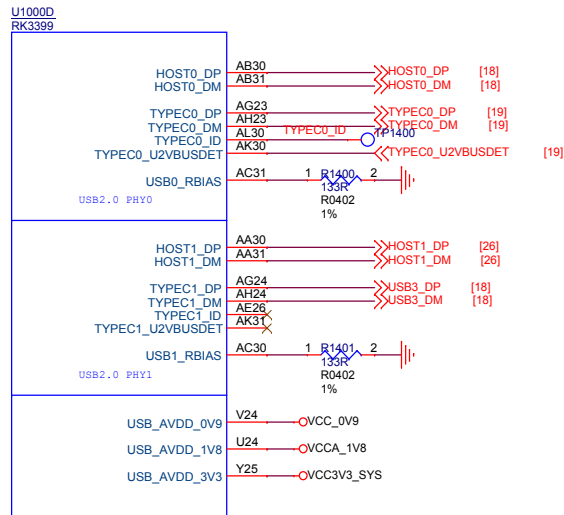
SDMMC design rule:
1. Data[0:3]、cmd 线做为一组，
并行走线并包地，组内等长要求为+/-100 mil；
2. Clk 需要独走线并包地处理，与data间的
延时小于 2ps；
3. Max trace length < 3.93 inches；
4. Trace impedance 50ohm+/-10%；
5. 与其他信号间距遵循 3W 原则；



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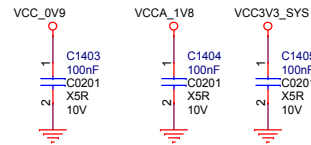
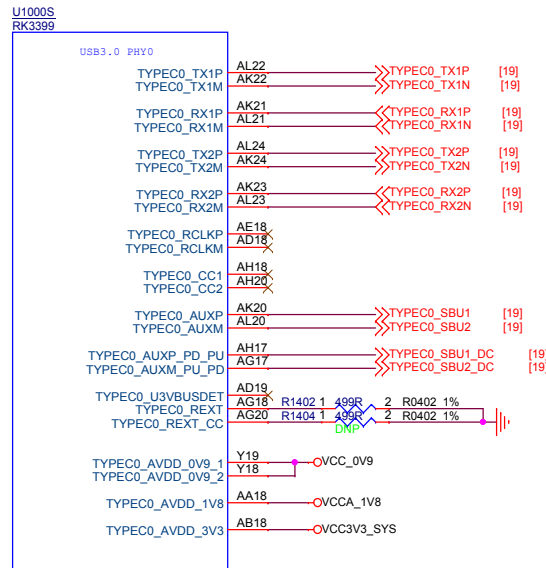


USB2.0

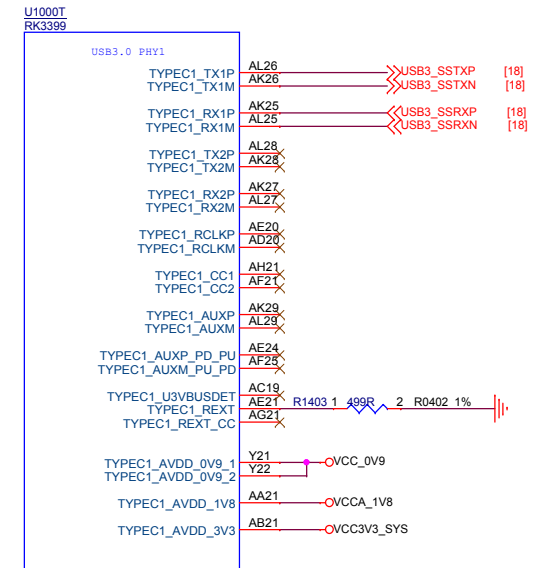


USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inches;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循 3原则;

USB3.0

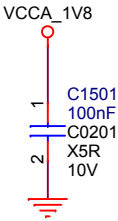
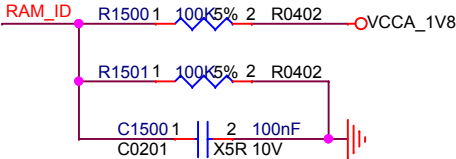
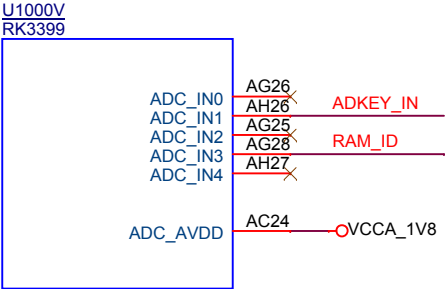


USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and RX < 1.6 ns;
3.Max trace length < 6 inches;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6. 与其他信号间距遵循 3原则;



DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inches;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循 3原则;

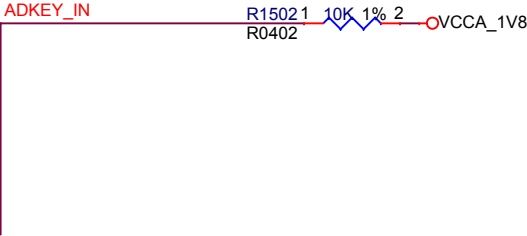
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	RAM ID	R1501 PU	R1502 PD
DDR3/DDR3L	0.6V	200K	100K
LPDDR3	0.112V	150K	10K
LPDDR4	1.5V	100K	499K

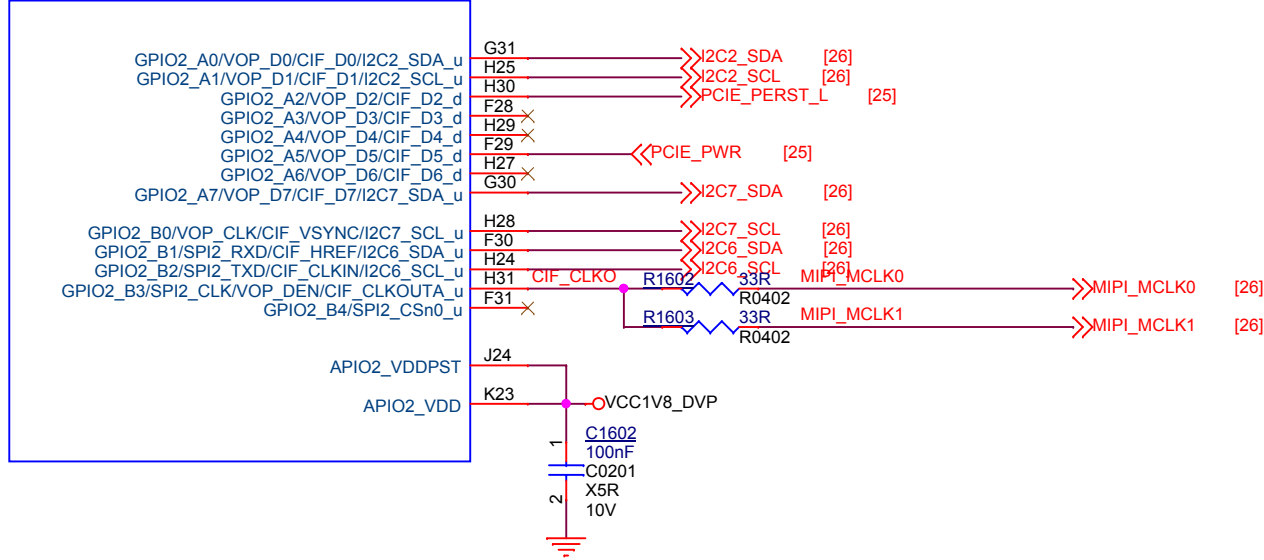
KEY BAORD

Note:
系统上电时，如果ADKEY_IN电平为0V，
则RK3399进入Recovery模式；
测量时 R1503, SW1500, ED1500 可以不 用贴片。

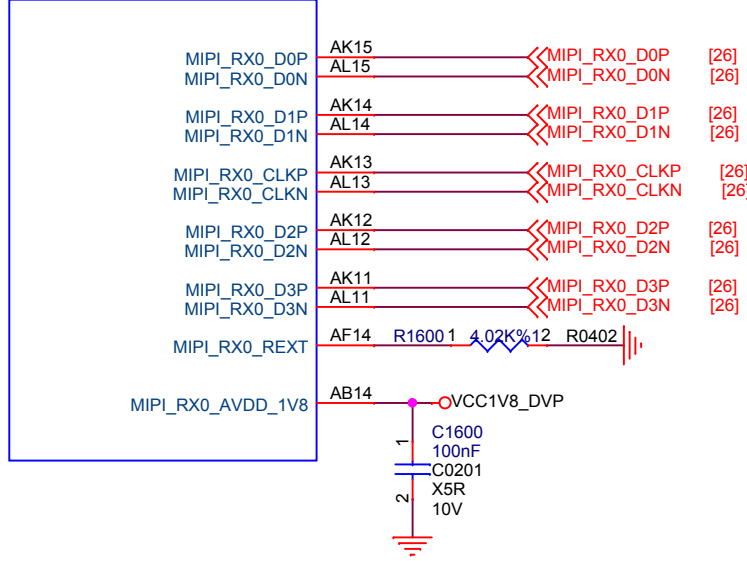


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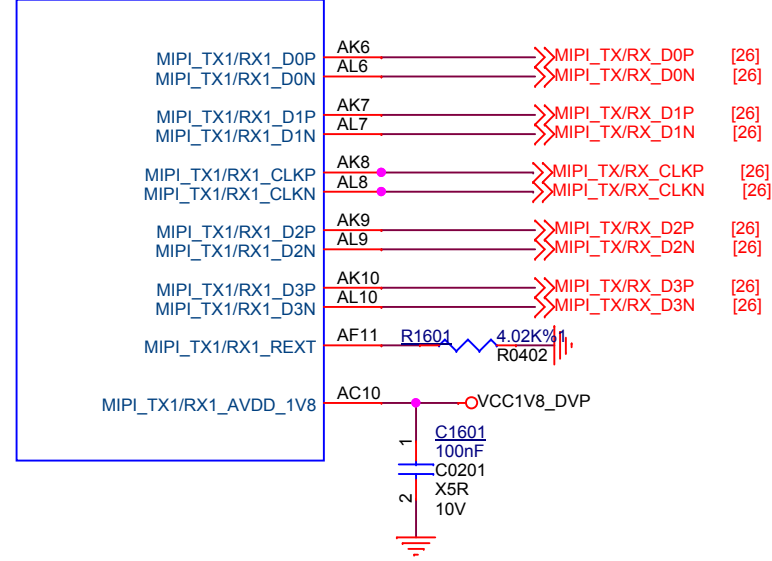
U1000L
RK3399



U1000R
RK3399

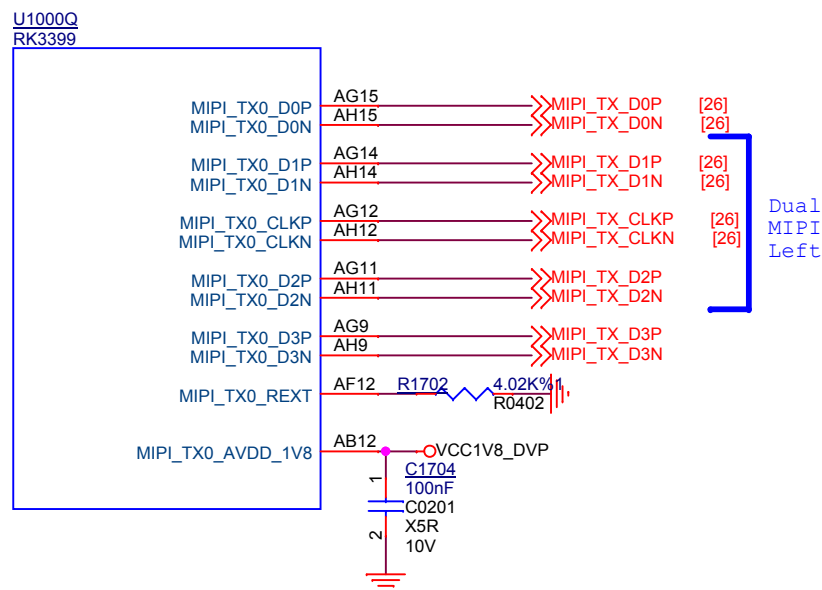
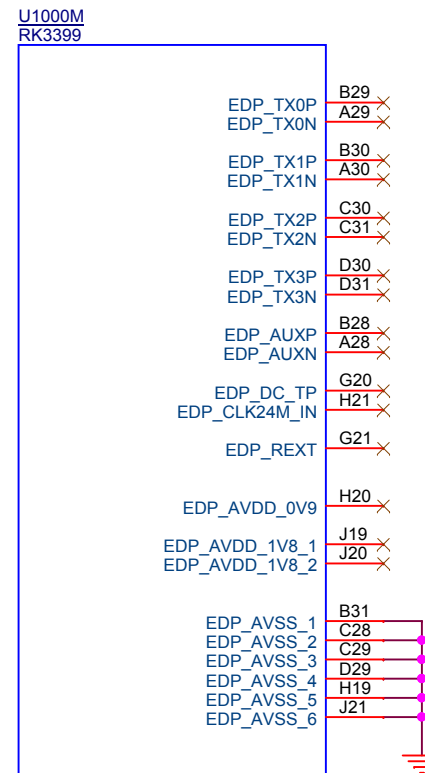
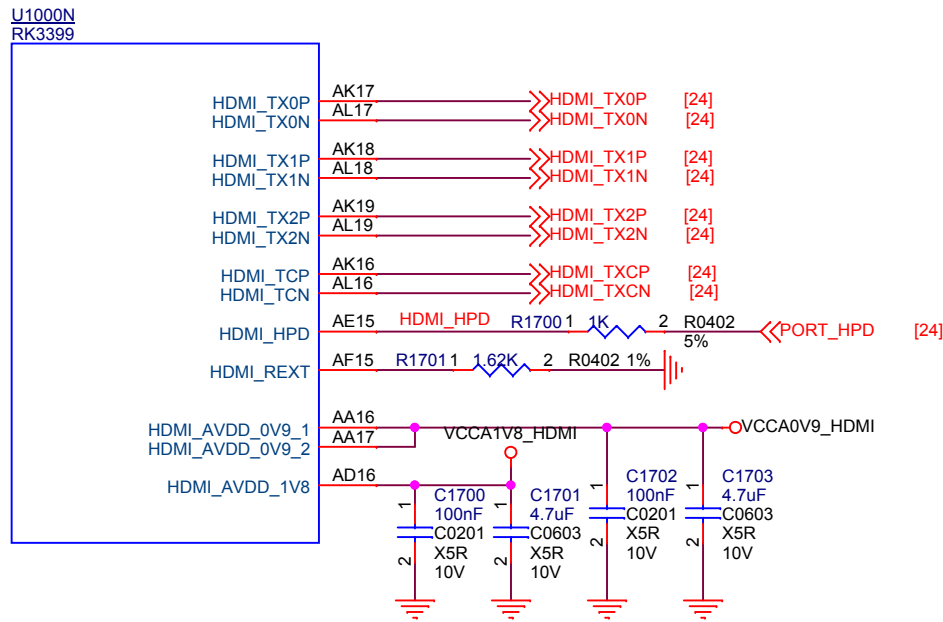


U1000P
RK3399



Dual
MIPI
Right

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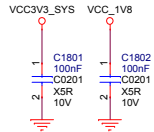


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U1000U Note:RK3399 part I is 3.3V only

GPIO3_A0/MAC_TXD2/SPI4_RXD_d
GPIO3_A1/MAC_TXD3/SPI4_TXD_d
GPIO3_A2/MAC_RXD2/SPI4_CLK_u
GPIO3_A3/MAC_RXD3/SPI4_CSn0_u
GPIO3_A4/MAC_TXD0/SPI0_RXD_d
GPIO3_A5/MAC_TXD1/SPI0_TXD_d
GPIO3_A6/MAC_RXD0/SPI0_CLK_u
GPIO3_A7/MAC_RXD1/SPI0_CSn0_u
GPIO3_B0/MAC_MDC/SPI0_CSn1_u
GPIO3_B1/MAC_RXDV_d
GPIO3_B2/MAC_RXER12C5_SDA_u
GPIO3_B3/MAC_CLK12C5_SCL_u
GPIO3_B4/MAC_TXEN/UART1_RX_u
GPIO3_B5/MAC_MDIO/UART1_TX_u
GPIO3_B6/MAC_RXCLK/UART3_RX_u
GPIO3_B7/MAC_CRS/CIF_CLKOUT/UART3_TX_u
GPIO3_C0/MAC_C0/UART3_CTSn/SPDIF_TX_u
GPIO3_C1/MAC_TXCLK/UART3_RTSn_u

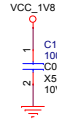
API01_VDDPST
API01_VDD



U1000G Note:RK3399 part G is 1.8V only

GPIO2_C0/UART0_RX_u
GPIO2_C1/UART0_TX_u
GPIO2_C2/UART0_CTSn_u
GPIO2_C3/UART0_RTSn_u
GPIO2_C4/SDIO0_D0/SPI5_RXD_u
GPIO2_C5/SDIO0_D1/SPI5_TXD_u
GPIO2_C6/SDIO0_D2/SPI5_CLK_u
GPIO2_C7/SDIO0_D3/SPI5_CSn0_u
GPIO2_D0/SDIO0_CMD_u
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u
GPIO2_D2/SDIO0_DET/PCIE_CLKREQn_d
GPIO2_D3/SDIO0_PWREN_d
GPIO2_D4/SDIO0_BKPPWR_d

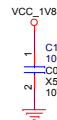
API03_VDD1V8



U1000J Note:RK3399 part J is 1.8V/3.0V mode

GPIO3_D0/I2S0_SCLK_d
GPIO3_D1/I2S0_LRCK_RX_d
GPIO3_D2/I2S0_LRCK_TX_d
GPIO3_D3/I2S0_SDIO_d
GPIO3_D4/I2S0_SDIO0_D3
GPIO3_D5/I2S0_SDIO2_D2
GPIO3_D6/I2S0_SDIO3_D1_d
GPIO3_D7/I2S0_SDIO0_d
GPIO4_A0/I2S0_CLK_d
GPIO4_A1/I2C1_SDA_u
GPIO4_A2/I2C1_SCL_u
GPIO4_A3/I2S1_SCLK_d
GPIO4_A4/I2S1_LRCK_RX_d
GPIO4_A5/I2S1_LRCK_TX_d
GPIO4_A6/I2S1_SDIO_d
GPIO4_A7/I2S1_SDIO0_d

API05_VDDPST
API05_VDD

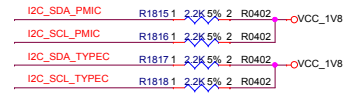
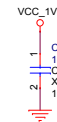


U1000E Note:RK3399 part E is 1.8V/3.0V mode

GPIO1_A0/SP0_SHUTTER_EN/ISP1_SHUTTER_EN/TPCD_VBUS_SINK_EN_d
GPIO1_A1/SP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TPCD_C03_VCONN_EN_d
GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TPCD_C01_VCONN_EN_d
GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_d
GPIO1_A4/SP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_d
GPIO1_A5/AP_PWROFF_d
GPIO1_A6/TSADC_INT_z
GPIO1_A7/SP1_RXD/UART4_RX_u
GPIO1_B0/SP1_TXD/UART4_TX_u
GPIO1_B1/SP1_CLK/PMCU_JTAG_TCK_u
GPIO1_B2/SP1_CSn0/PMCU_JTAG_TMS_u
GPIO1_B3/I2C4_SDA_u
GPIO1_B4/I2C4_SCL_u
GPIO1_B5_d
GPIO1_B6/PMW0B_IR_d
GPIO1_B7/SP13_RXD/I2C0_SDA_u
GPIO1_C0/SP13_TXD/I2C0_SCL_u
GPIO1_C1/SP13_CLK_d
GPIO1_C2/SP13_CSn0_u
GPIO1_C3/PMW2_d
GPIO1_C4/I2C8_SDA_u
GPIO1_C5/I2C8_SCL_u
GPIO1_C6/TPCD_VBUS_SOURCE0_d
GPIO1_C7/TPCD_VBUS_SOURCE1_d
GPIO1_D0/TPCD_VBUS_SOURCE2_d
DFTJTAG_TMS_u
DFTJTAG_TRSTn_d

PMUIO2_VDDPST
PMUIO2_VDD

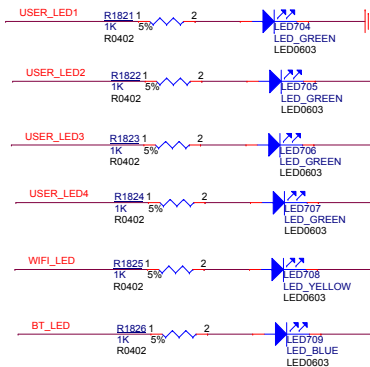
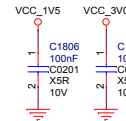
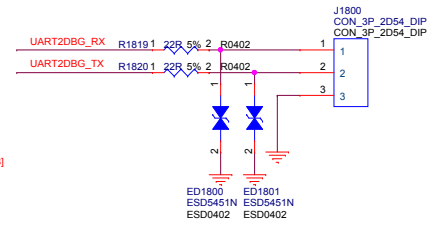
1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
other	3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V



U1000K Note:RK3399 part J is 1.8V/3.0V mode

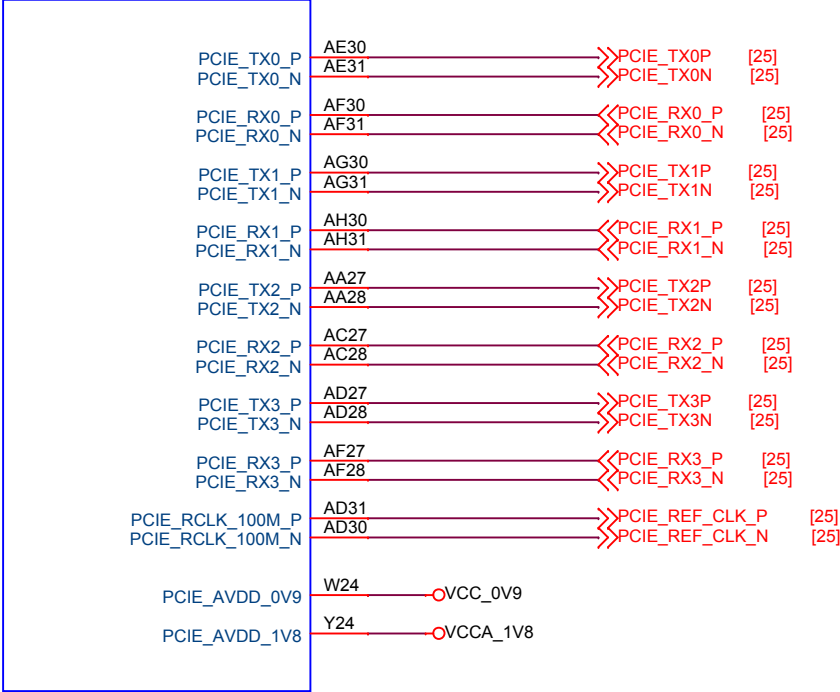
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GPIO4_C1/I2C3_SCL/UART2B_TX_u
GPIO4_C2/PMW0VOP0_PWMVOP1_PWM_d
GPIO4_C3/UART2C_RX_u
GPIO4_C4/UART2C_TX_u
GPIO4_C5/SPDIF_TX_d
GPIO4_C6/PMW1_d
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u
GPIO4_D0/PCIE_CLKREQn8_u
GPIO4_D1/DP_HOTPLUG_d
GPIO4_D2_d
GPIO4_D3_d
GPIO4_D4_d
GPIO4_D5_d
GPIO4_D6_d

API04_VDDPST
API04_VDD



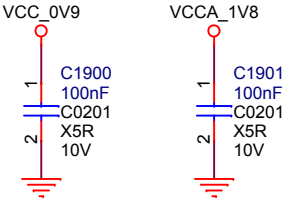
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U1000Q
RK3399



PCIE design rule:

- 1.Max intra-pair skew < 4ps;
- 2.Max inter-pair skew < 1.6 ns;
- 3.Max trace length < 14 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循 3W原则 ;



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DC IN&SYSTEM Power

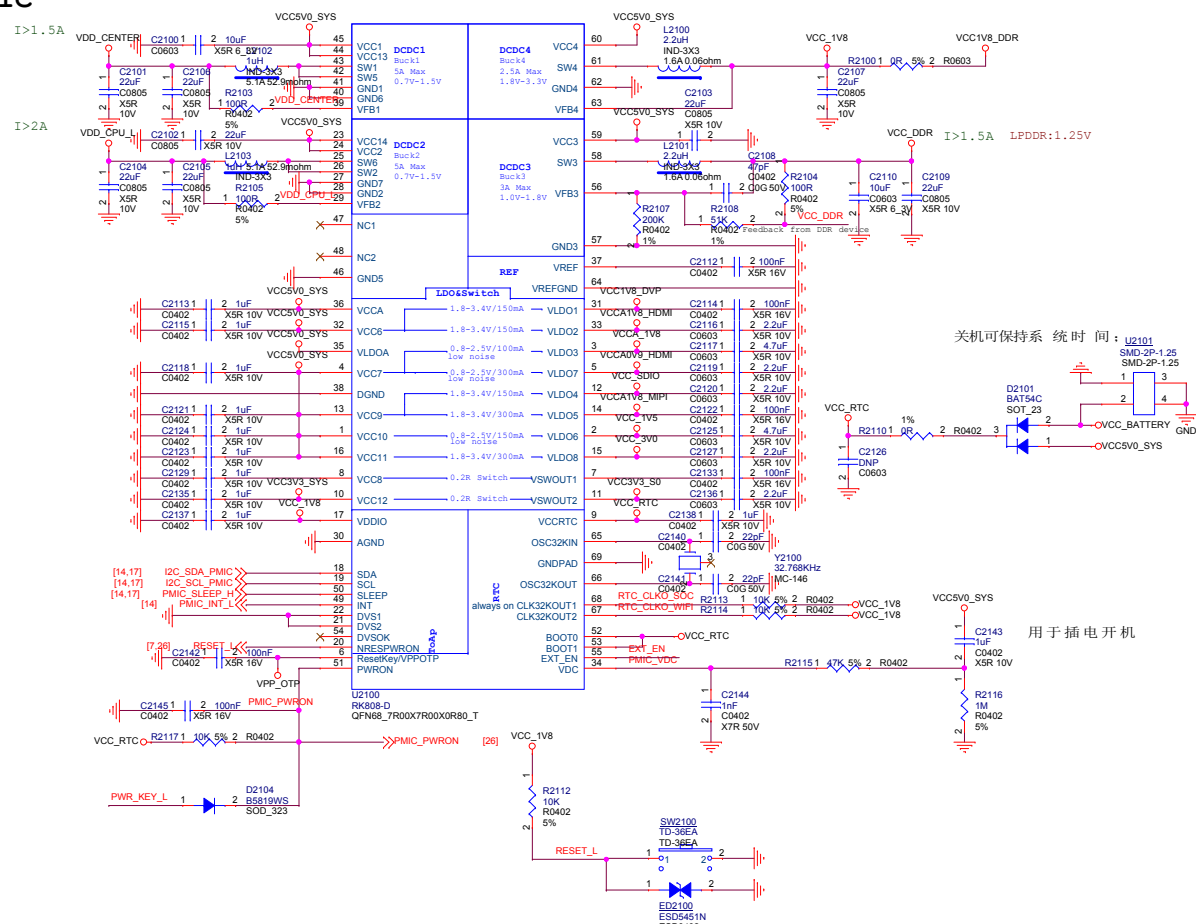
The schematic illustrates a DC power conversion system with two buck converter stages. The input is VCC12V_DCIN, which is connected to VCC12V. The first stage (U2000, SY8113B) converts VCC12V to VCC5V0_SYS (5.1V/3A). The second stage (U2001, SY8113B) converts VCC12V to VCC5V0_USB (5.1V/3A). Both stages include input capacitors (C2002, C2003, C2009, C2010), a 10K resistor (R2001, R2005), a 100nF capacitor (C2000, C2008), an inductor (L2000, L2001), and output capacitors (C2004, C2005, C2006, C2007, C2011, C2012, C2013, C2014). The schematic also shows a diode (D2000) and a MOSFET (M2000) for the first stage.

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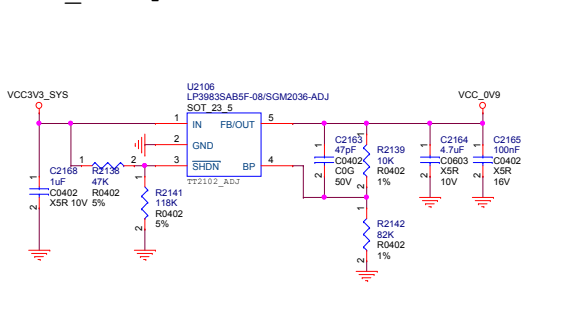
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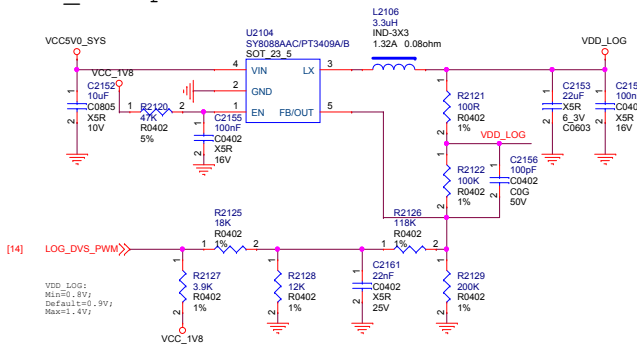
PMIC



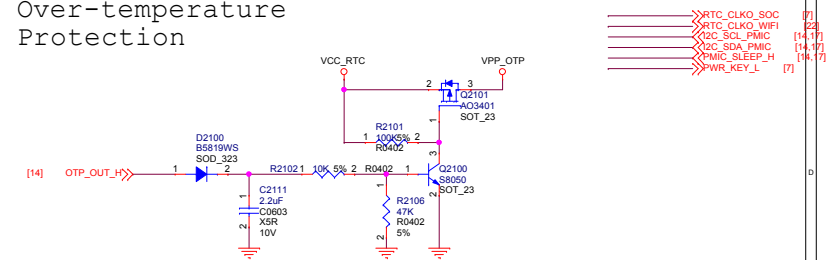
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VCC 0V9 power
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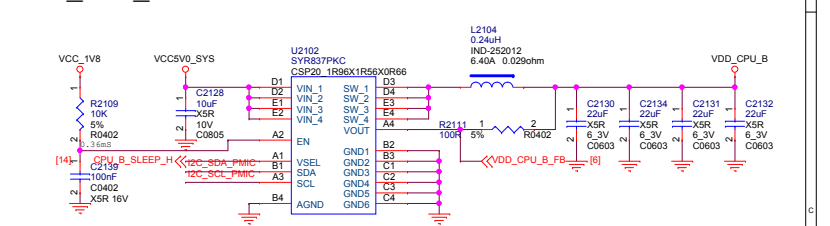
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VDD LOG power
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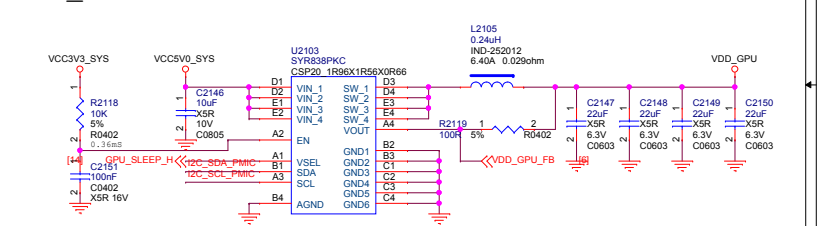
Over-temperature Protection



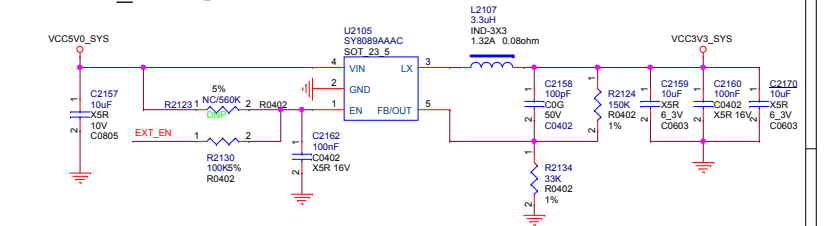
VDD_CPU_B power



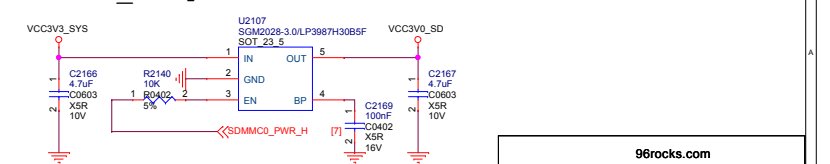
VDD_GPU power



VCC3V3 SYS power

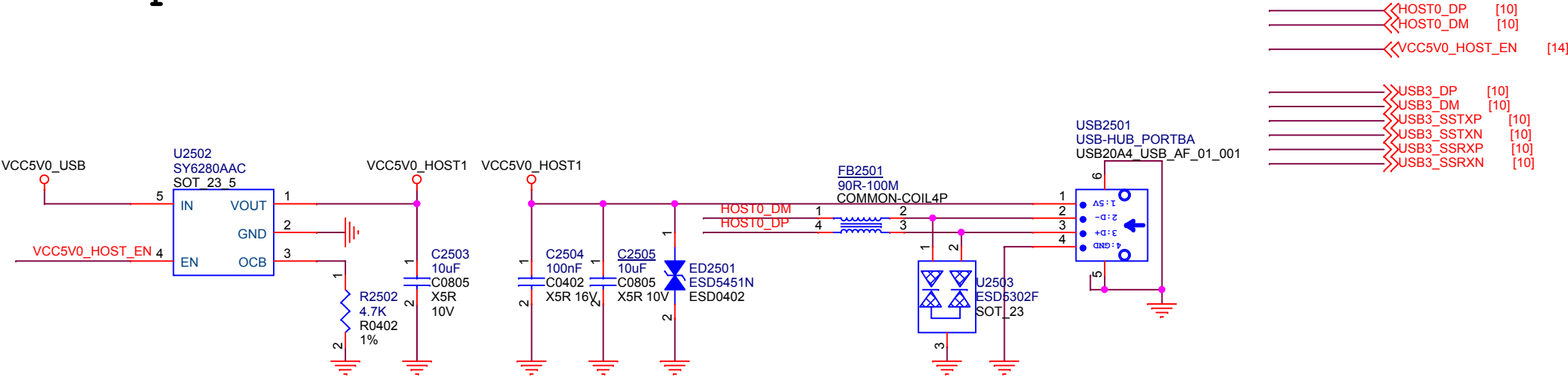


VCC3V0 SD power

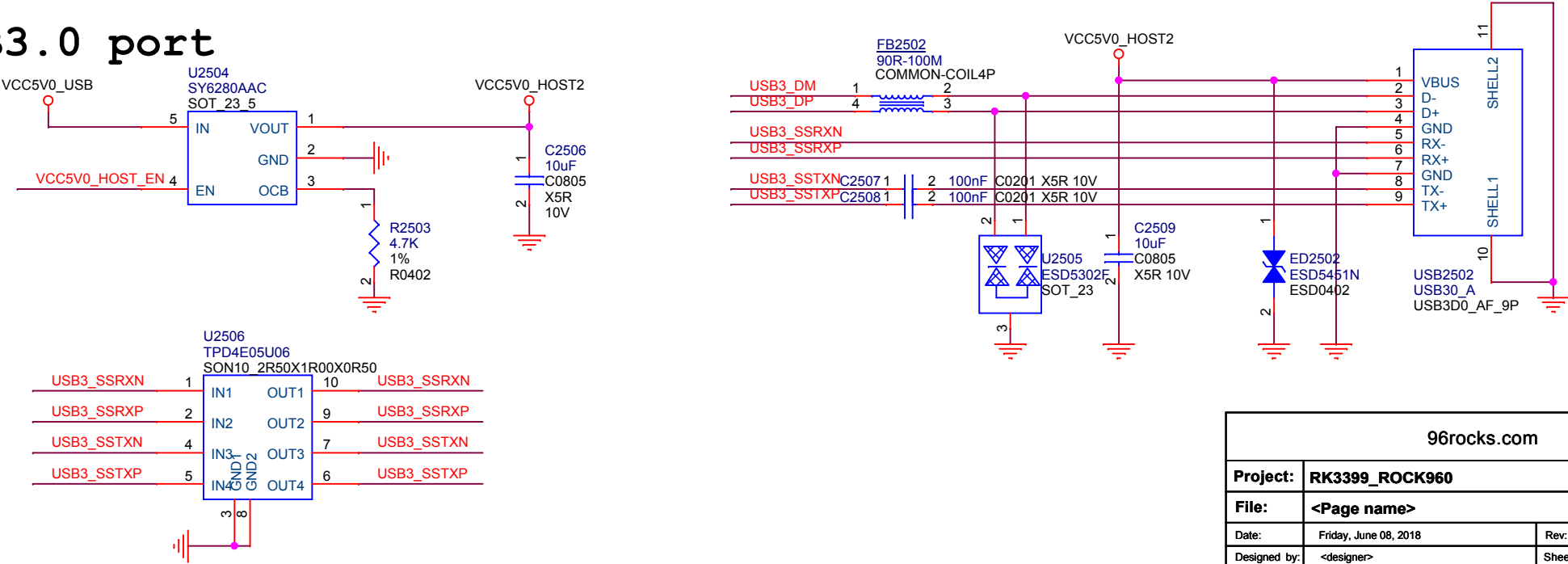


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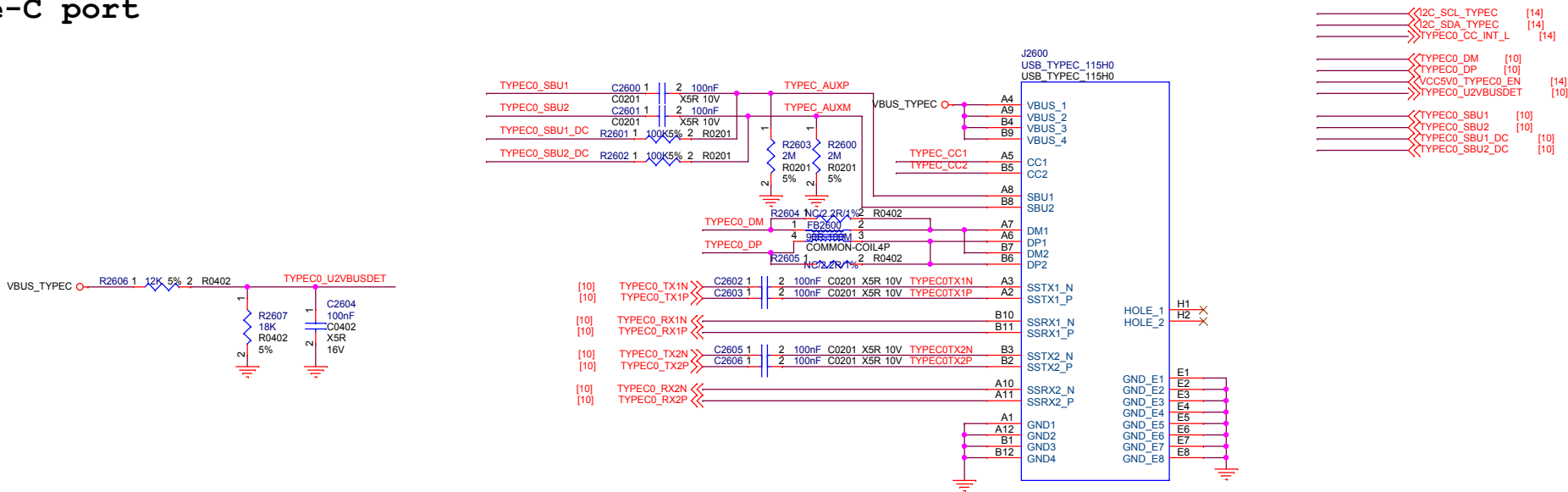
USB2.0 port



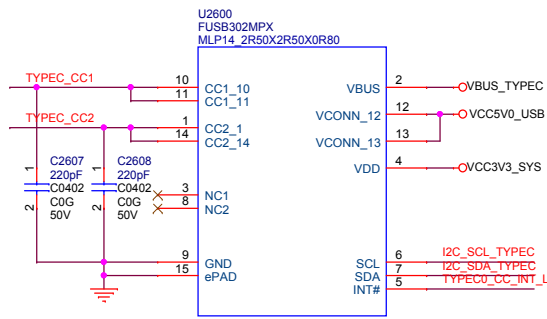
USB3.0 port



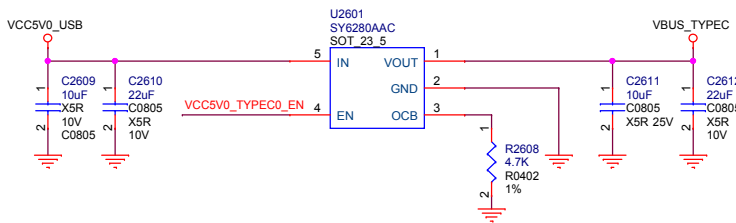
USB Type-C port



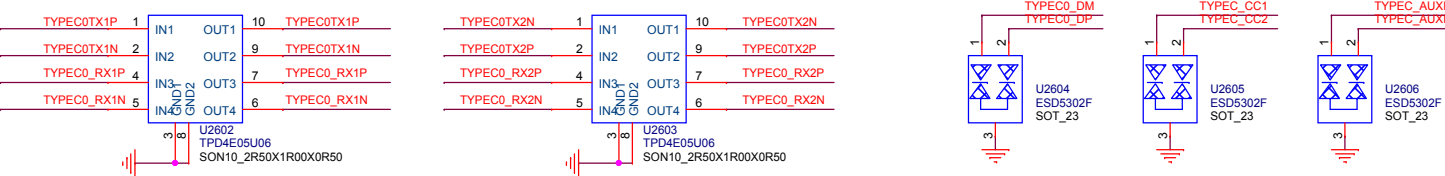
CC CTRL



Limit switch

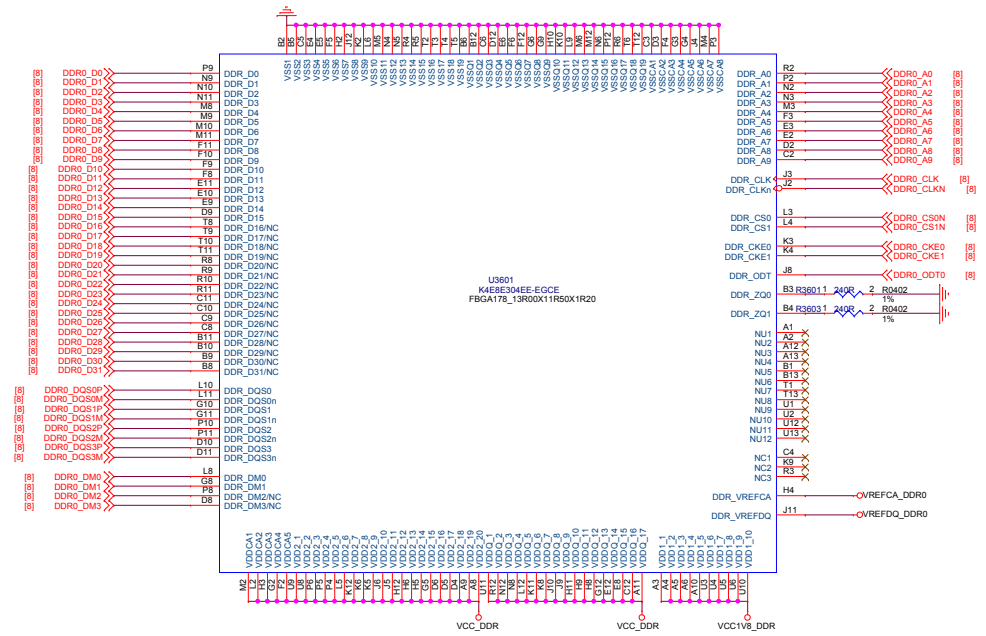
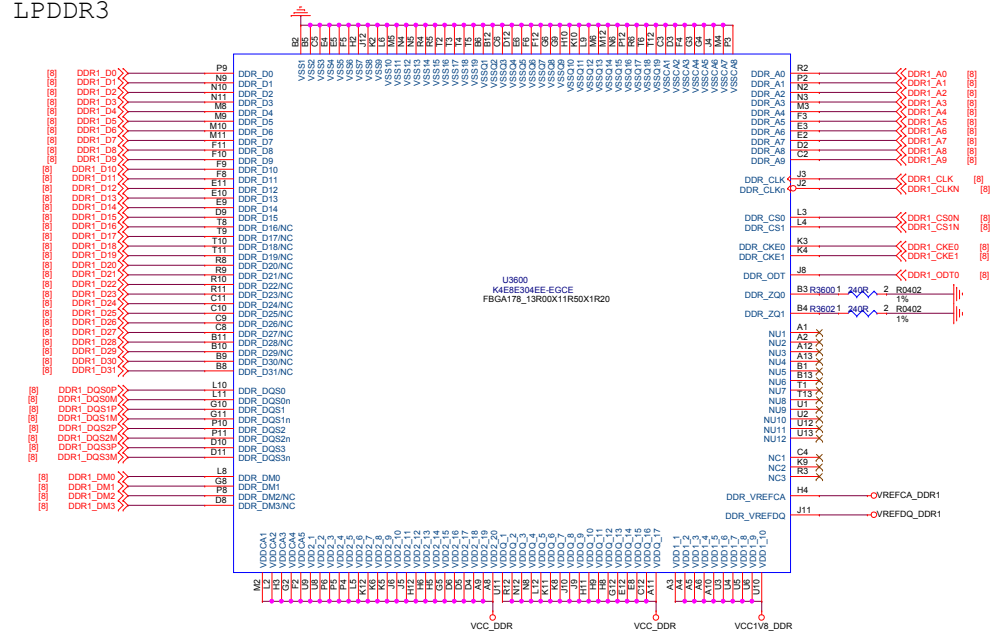


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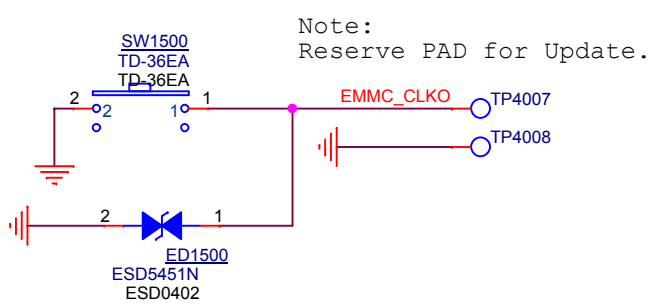
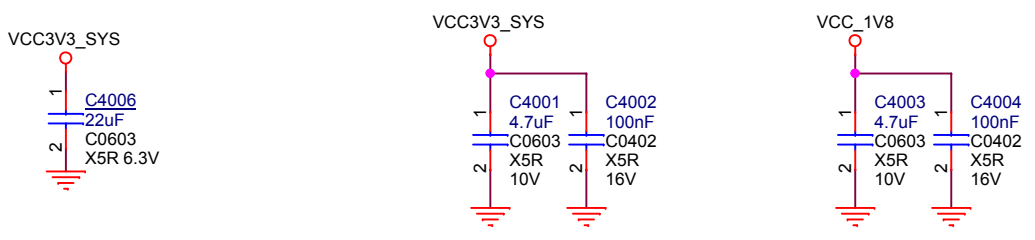
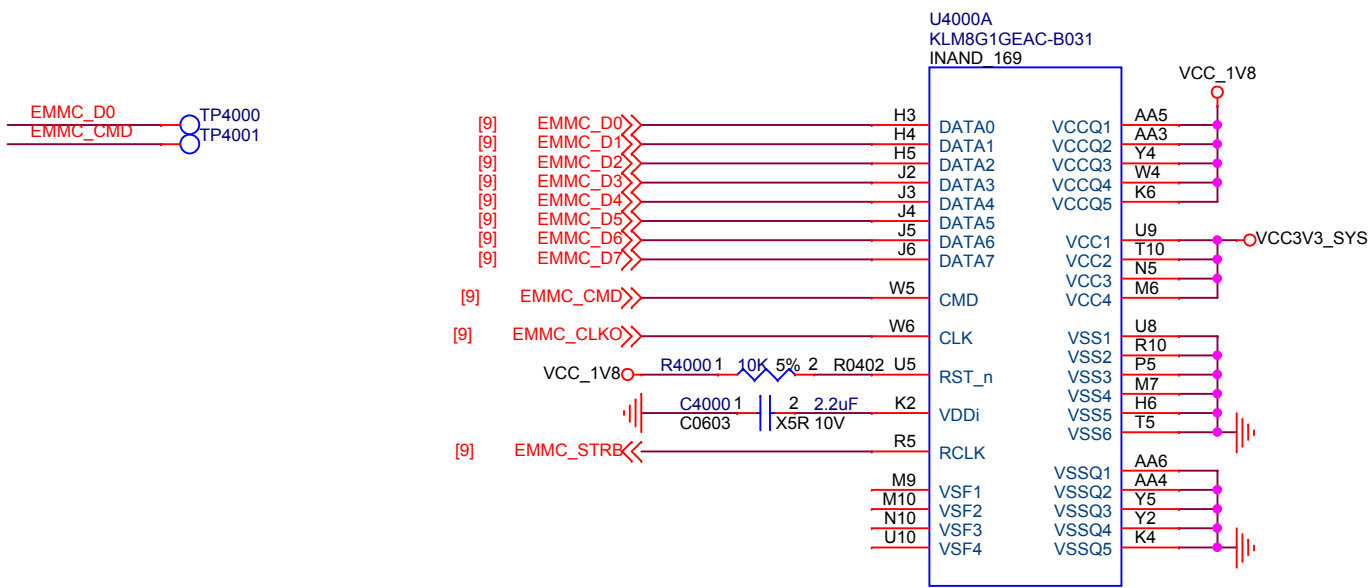


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LPDDR3

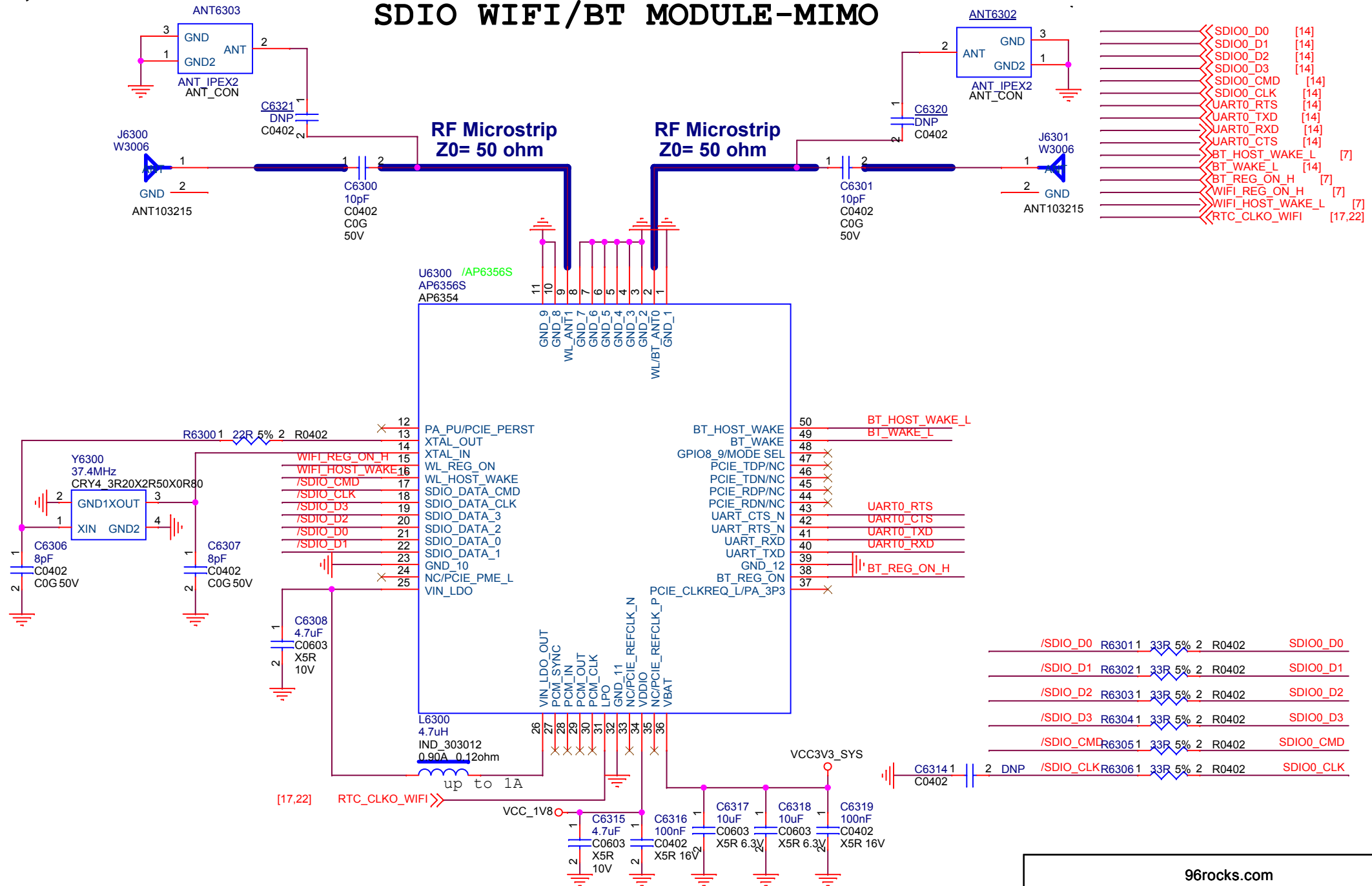


eMMC FLASH



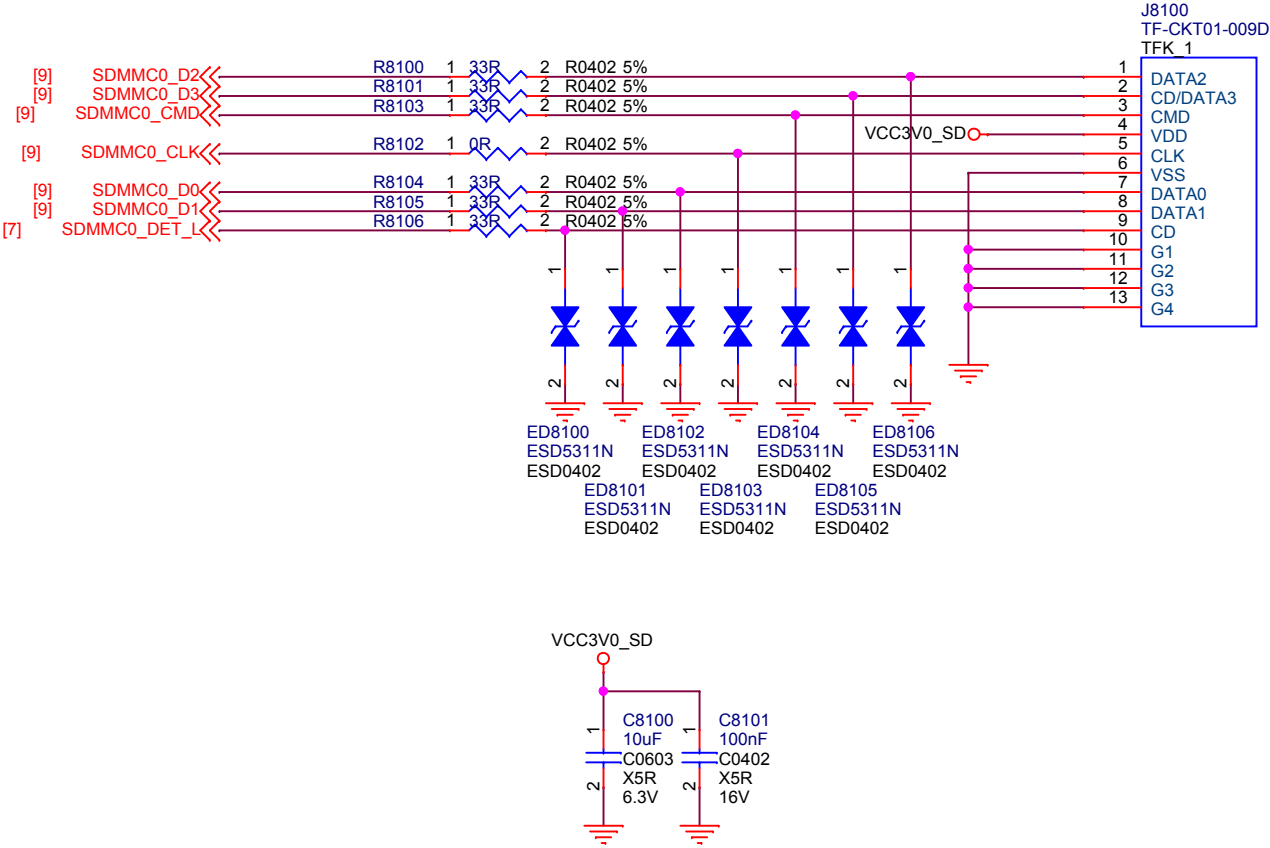
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SDIO WIFI/BT MODULE-MIMO



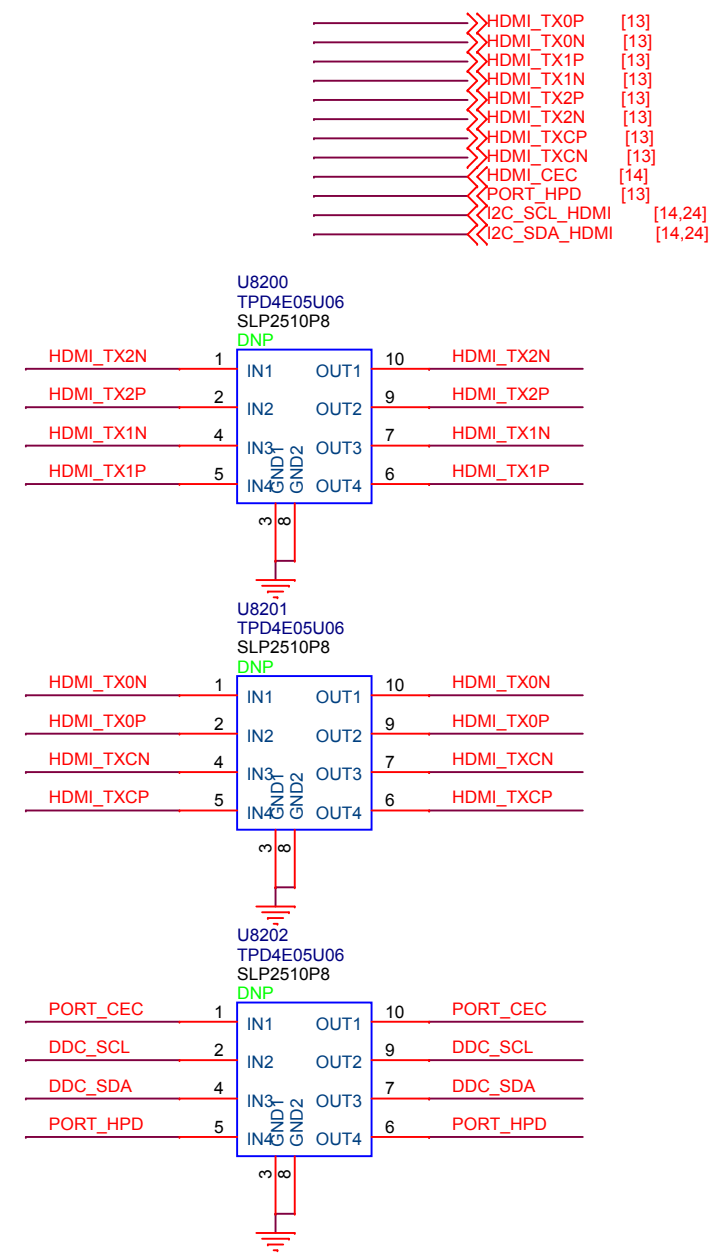
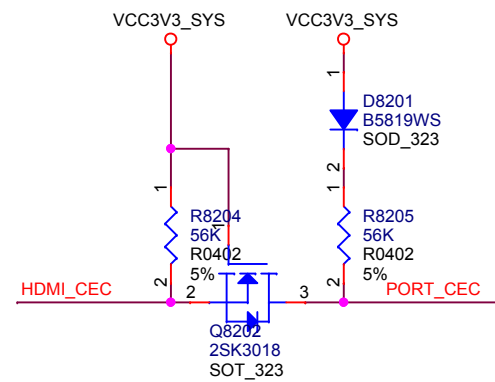
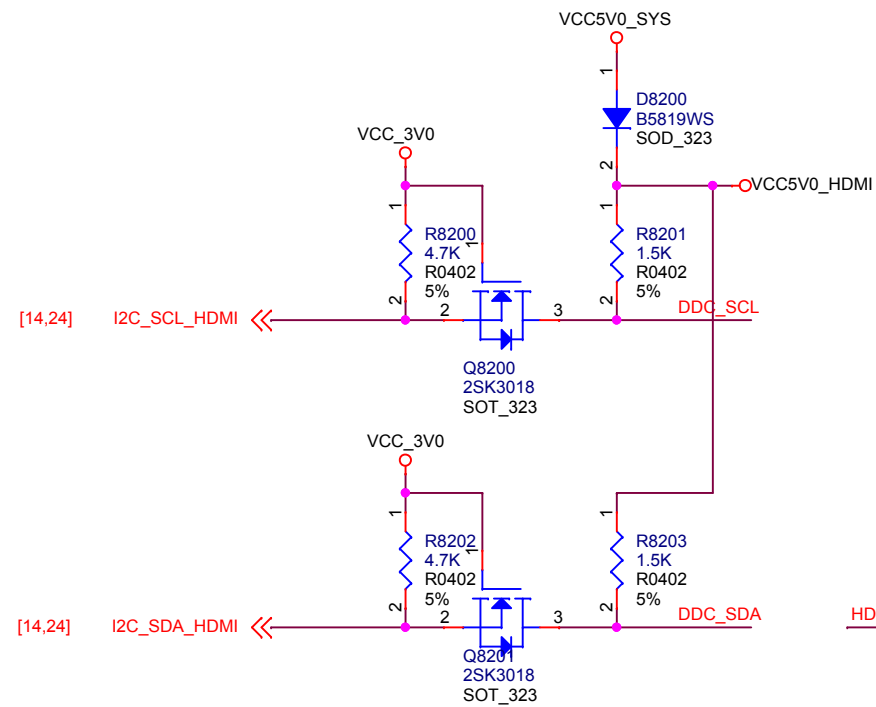
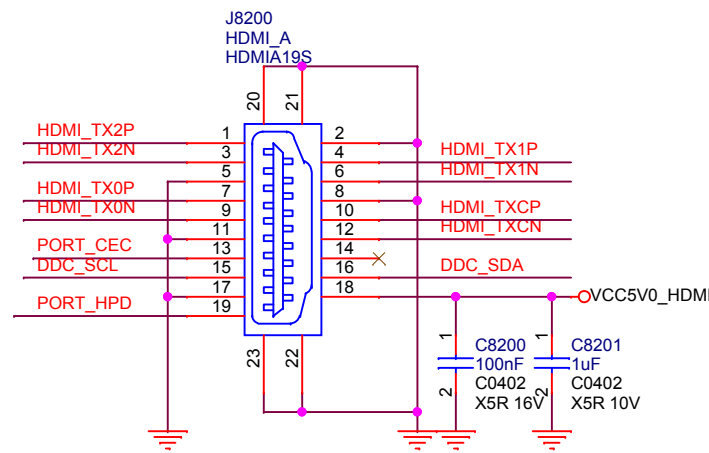
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TF CARD



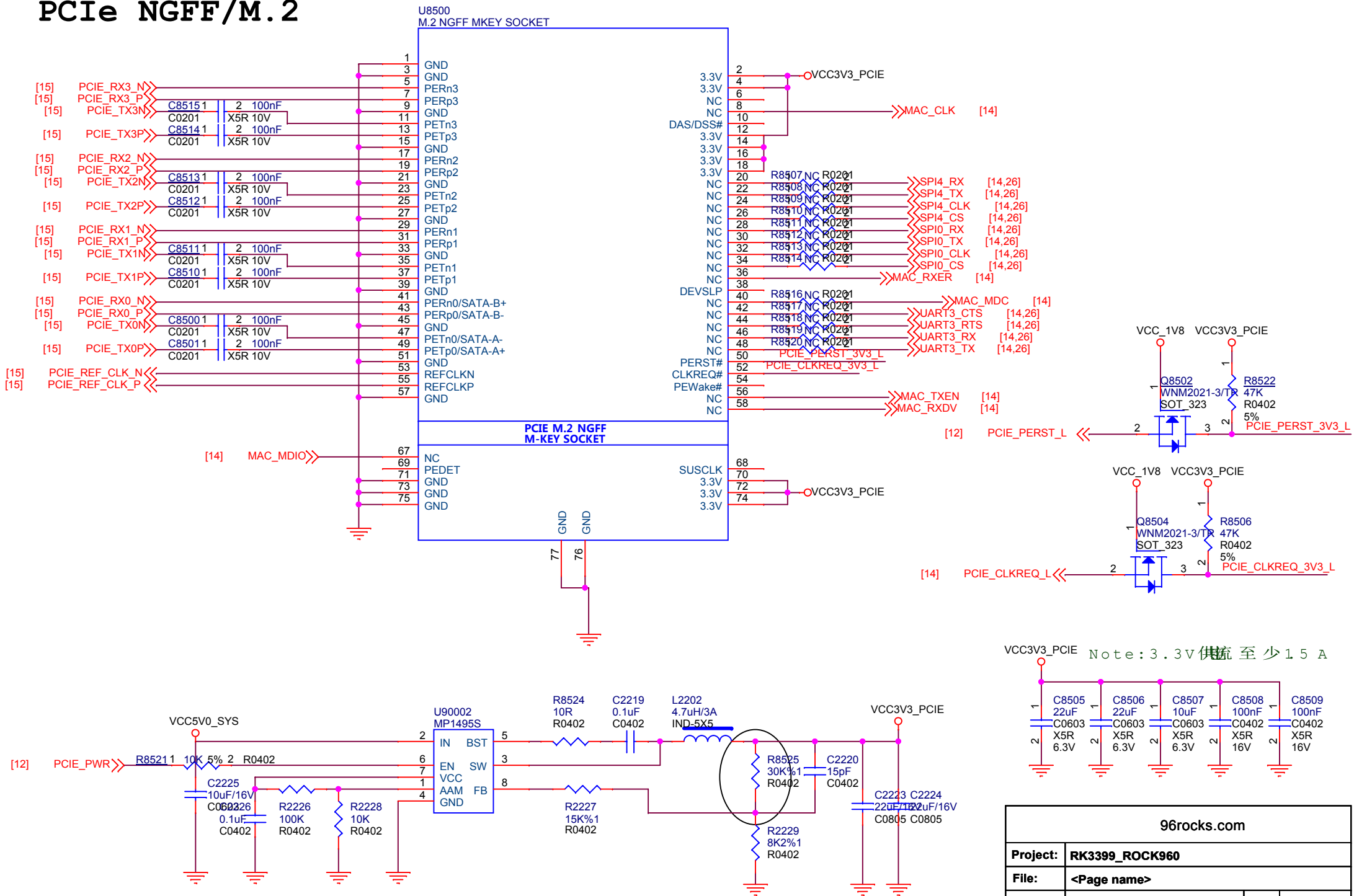
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HDMI Output



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PCIe NGFF/M.2



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注意：
电压VCCB>=VCA。

