Power Management System Technical Specifications

PRELIMINARY

V1.0.1

2015-1-5

Fuzhou Rockchip Electronics Co.Ltd

REVISION HISTORY

Date	Revision	Description
2013-03-02	0.1	Initial preliminary version
2013-03-25	0.2	Initial complete version
2013-08-31	0.3	Updated register map
2013-12-4	0.4	Changed package information
2014-02-22	0.5	Changed some details information
2014-03-14	0.6	Adding some information
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2014-09-13	0.8	1.revised the packaging information 2.adding the BOOT11 timing sequence 3.Revised the BUCK1/2 output voltage range from 0.7v~1.5v to 0.7125v~1.5V
2014-12-30	1.0	1. adding ordering information for RK808-B/RK808-C 2.adding BOOT11 start up sequence of RK808-B/RK808-C 3. adding
2014-01-05	1.0.1	1.changing the BUCK1/BUCK2 Output voltage transition rate

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1 OVERVIEW

The RK808 is a complete power supply solution for Portable systems. The highly integrated device includes four buck DC-DC converters, eight high performance ldos, two low Rds switches, I^2C interface, programmable power sequencing and an RTC.

The RK808 improves performance, reduces component count and size, and therefore provides lower cost solution compared to conventional portable designs. The ultra fast 2MHz current mode DC/DC architecture optimizes the transient performance and is compatible with tiny low cost ceramic inductors and capacitors. All DC/DC channels include integrated MOSFETS. Internal soft-start and compensation circuits minimize external components count. Most outputs can be programmed through the I^2C interface

2 FEATURES

- Input voltage range: 2.7V to 5.5V
- 2MHz Switching Frequency for bucks
- Current mode architecture for best transient performance
- Internal compensation and soft start
- I^2C Programmable output levels and power sequencing
- High efficiency architecture
- Integrated Vout Discharge Circuit for BUCK and LDO
- Power:
  - CH1: Synchronous Buck regulator, 5A max
  - CH2: Synchronous Buck regulator, 5A max
  - CH3: Synchronous Buck regulator, 3A max
  - CH4: Synchronous Buck regulator, 2.5A max
  - CH6,CH7,CH9,CH11: Linear regulators, 150mA max
  - CH8: Low noise and high PSRR linear regulator,100mA max
  - CH10,CH12,CH13: Linear regulators, 300mA max
  - CH14: Low Rds switch, 0.2ohm@Vgs=3v
  - CH15: Low Rds switch, 0.2ohm@Vgs=3v
- Auxiliary: Flexible Power Sequence control
- Package: 7mmx7mm QFN68

3 BLOCK DIAGRAM

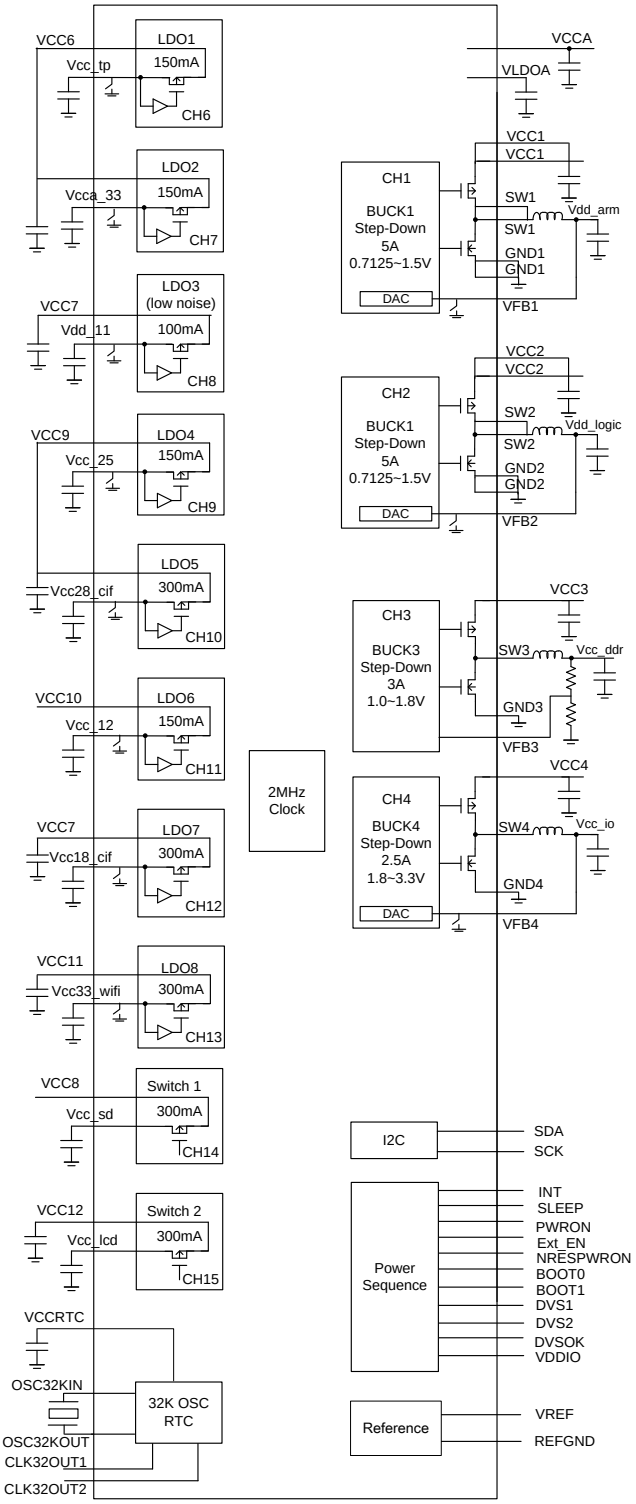


Figure 3-1 Functional Block Diagram

4 TYPICAL APPLICATION DIAGRAMS

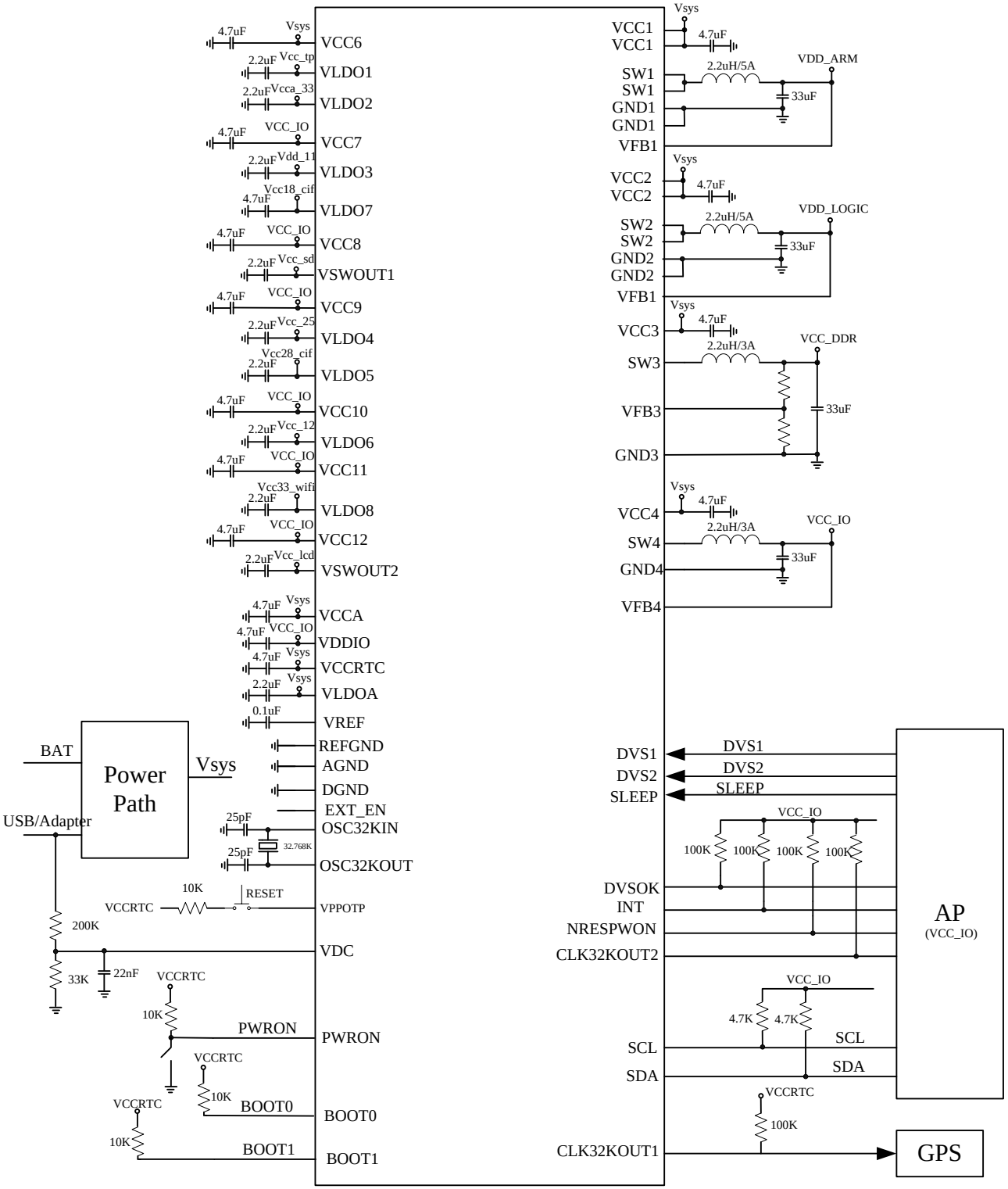


Figure 4-1 RK808 One Battery Cell Application

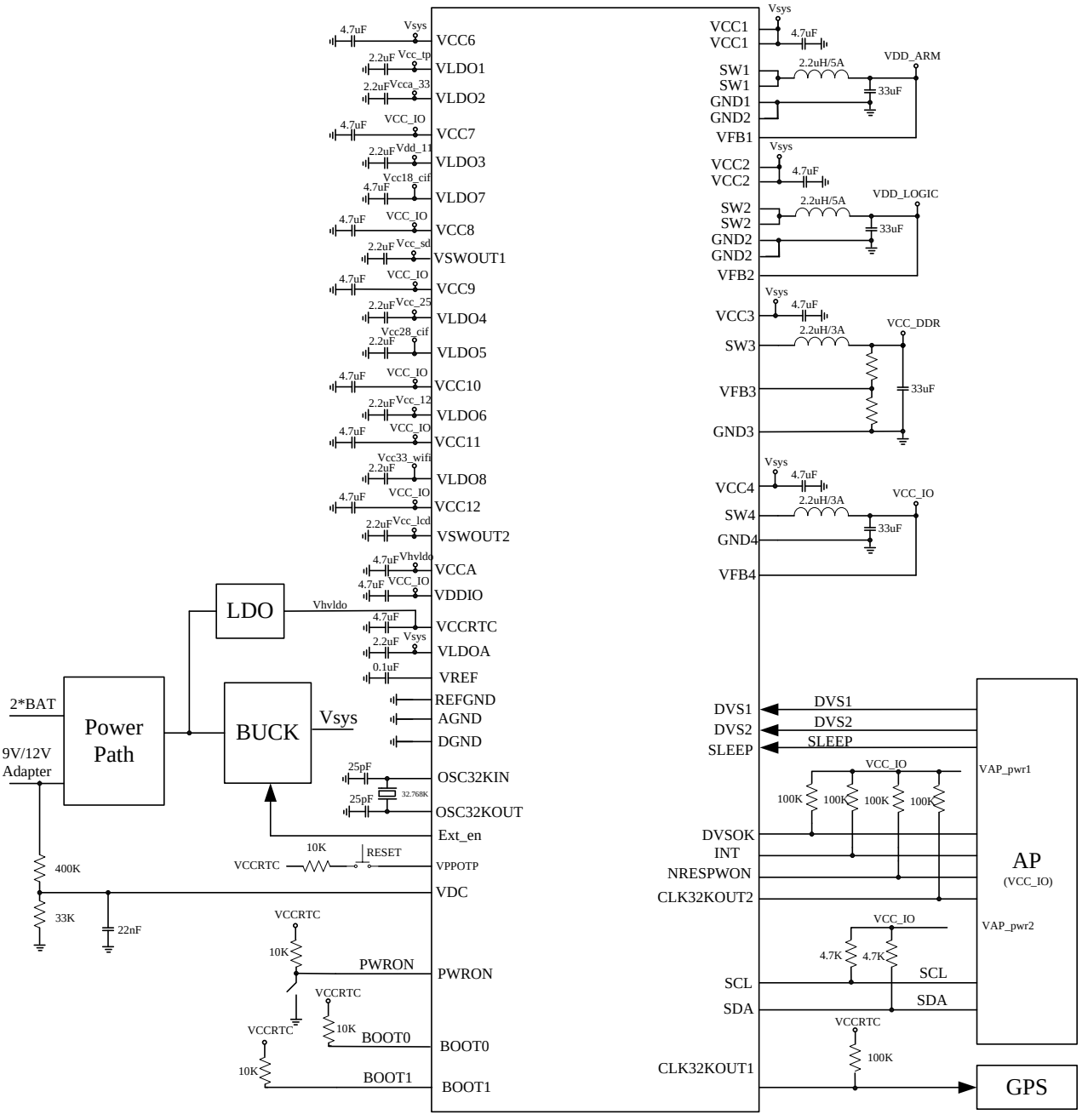


Figure 4-2 RK808 Two Battery Cells Application

5 ORDERING INFORMATION

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RK808-B	RoHS pass	QFN68(7X7)	2600ea/inner box* 6 inner boxes/outer box	For RK3288 B-application
RK808-C	RoHS pass	QFN68(7X7)	2600ea/inner box* 6 inner boxes/outer box	For RK3288 C-application

6 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Voltage range on pins VCCx, VDDIO, VCCRTC, VFBx, VLDOx, VSWOUTx, VREF	-0.3	7	V
Voltage range on pin CLK32KOUT1, CLK32KOUT2, VDC, SLEEP	-0.3	7	V
Voltage range on pins OSC32KIN, OSC32KOUT, BOOT0, BOOT1, EXT_EN, PWRON	-0.3	$VCCRTC_{MAX}$+0.3	
Voltage range on pins NRESPWRON, INT, SDA, SCL, DVS1, DVS2, DVSOK	-0.3	VDDIO+0.3	V
Storage temperature range, T_S	-40	150	℃
Operating temperature range, T_J	-40	125	℃
Maximum Soldering Temperature, T_{SOLDER}		300	℃

Note 1. Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

7 RECOMMENDED OPERATING CONDITIONS

Parameter	Min	TYP	Max	Units
Voltage range on pins VCCx, VDDIO	3		5.5	V
Voltage range on pin VCCRTC	2.5		5.5	V
Voltage range on other pins			5.5	V
Power Dissipation			2.5	W

8 ELECTRICAL CHARACTERISTICS

T_J=25C; V_{BAT}=VCCx=3.8V, VDDIO=3V unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
General					
Input supply voltage range (VBAT)	V_{INPUT}	2.7		5.5	V
Battery low alarm voltage (2.8V~3.5V programmable, step=100mV)	V_{BLO}	3.25	3.3	3.35	V
Battery under voltage threshold (vin falling)	V_{BUVL}		2.5		V
Battery under voltage threshold (vin rising)	V_{BUVH}	2.6	2.7	2.8	V
Battery OK voltage threshold （3.0V/3.4V/3.5V/3.6V OTP programmable）	V_{BOK}		3.0		V
Power on Reset Threshold (Rising)	V_{PORH}			2.2	V
Power on Reset Threshold (Falling)	V_{PORL}	1.2			V
Over Voltage Lock Out Threshold (Vin Rising)	$V_{TH(OVLO)}$	5.7	6.0	6.3	V
Over Voltage Lock Out Hysteresis	$V_{HYS\ (OVLO)}$		0.2		V
VDC pin threshold(rising edge)	V_{DCH}		0.6		V
VDC pin threshold(falling edge)	V_{DCL}		0.54		V
Stand-by current, V_{DD}=3.6V, device OFF state 32KHz clock running	$I_{Q(STNBY)}$		60		uA
Hot-die temperature rising threshold (85℃~115℃ programmable, step=10℃)	T_{HD}	85		115	℃
Thermal shut down (140℃~170℃ programmable, step=30℃)	T_{TSD}	140		170	℃
Oscillator circuit					
Switching Frequency CH1,2,3,4(Tj=25℃)	f_{SW}	1.8	2	2.2	MHz
Logic inputs					
Input LOW-Level Voltage (V_{DDIO})	V_{IL}			0.3xV_{DDIO}	V
Input HIGH-Level Voltage (V_{DDIO})	V_{IH}	0.7xV_{DDIO}			V
Logic outputs					
LOW-Level Output Voltage, 3.0 mA sink current	V_{OL}			0.4	V
HIGH-Level Output Voltage, 3.0 mA source current	V_{OH}	V_{DDIO}-0.4			V
NRESPWON pin LOW-Level Output Voltage, 3.0mA sink current	$V_{OL(NRES)}$			0.4	V
CLK32KOUT1 pin LOW-Level Output Voltage,	$V_{OL(CLKO1)}$			0.4	V

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.0mA sink current					
CLK32KOUT2 pin LOW-Level Output Voltage, 3.0mA sink current	$V_{OL(CLKO2)}$			0.4	
CLK32KOUT2 pin HIGH-Level Output Voltage, 3.0mA source current	$V_{OH(CLKO2)}$	V_{DDIO}-0.4			V
CH1 Buck1 Regulator (VDD_ARM)					
Input supply voltage range	V_{INPUT1}	2.7		5.5	V
Voltage Adjustable Range, 6bit	V_{FB1}	0.7125		1.500	V
DC output voltage programmable step(DVS)			12.5		mV
Output voltage transition rate BUCK1_RATE=00 BUCK1_RATE=01 BUCK1_RATE=10 BUCK1_RATE=11			 2 3.6 5 6.5		mV/us
DVS OK threshold (Vout rising)	$V_{DVSOKR1}$		93		%
DVS OK threshold (Vout falling)	$V_{DVSOKF1}$		107		%
Power Good threshold (Vout rising)	V_{PG1}		93		%
Output under voltage lockout(Vout falling)	V_{UV1}		85		%
Output over voltage lockout (Vout rising)	V_{OV1}		117		%
Preset Voltage, Default(Tj=25℃)	$V_{FB1(Default)}$	1.078	1.100	1.122	V
Preset Voltage, Default(-10℃≦T_j≦+85℃)	$V_{FB1(Default)}$	1.067	1.100	1.133	V
Load Regulation, I_{OUT1} = 100mA to 5A			1		%/A
Line Regulation, VCC1 = 3 to 5V, I_{OUT1} = 1A			0.1		%/V
Rated output current(If I_{CL1}=6A)	I_{MAX1}		5		A
Switch Current Limit (4.5A~6A programmable, step=0.5A)	I_{CL1}		6		A
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q1}		70		uA
Minimun Switch Current Limit (50mA~400mA programmable, step=50mA)	I_{CLMIN1}		100		mA
Soft-start Time	t_{SS1}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS1}		250		ohm
Conversion Effeciency (Vin=3.8V,Vout=1.1V) Iout=5A Iout=4A Iout=3A Iout=2A Iout=1 A			 68 73 78 84 89		 %

Parameter	Symbol	Min.	Typ.	Max.	Unit
Iout=500mA			90		
Iout=100 mA			81		
Iout=10 mA			79		
CH2 Buck2 Regulator (VDD_LOG)					
Input supply voltage range	V_{INPUT2}	2.7		5.5	V_{INPUT2}
Voltage Adjustable Range, 6bit	V_{FB2}	0.7125		1.500	V_{FB2}
DC output voltage programmable step(DVS)			12.5		
Output voltage transition rate BUCK2_RATE=00 BUCK2_RATE=01 BUCK2_RATE=10 BUCK2_RATE=11			 2 3.6 5 6.5		
DVS OK threshold (Vout rising)	$V_{DVSOKR2}$		93		%
DVS OK threshold (Vout falling)	$V_{DVSOKF2}$		107		%
Power Good threshold (Vout rising)	V_{PG2}		93		%
Output under voltage lockout (Vout falling)	V_{UV2}		85		%
Output over voltage lockout (Vout rising)	V_{OV2}		117		%
Preset Voltage, Default(Tj=25℃)	$V_{FB2(Default)}$	1.078	1.100		V
Preset Voltage, Default(-10℃≦T_j≦+85℃)	$V_{FB2(Default)}$	1.067	1.100		V
Load Regulation, I_{OUT2} = 100 mA to 5A			1		%/A
Line Regulation, VCC2 = 3 to 5V, I_{OUT2} = 1A			0.1		%/V
Rated output current(If I_{CL2}=6A)	I_{MAX2}		5		A
Switch Current Limit (4.5A~6A programmable, step=0.5A)	I_{CL2}		6		A
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q2}		70		uA
Minimun Switch Current Limit (50mA~400mA programmable, step=50mA)	I_{CLMIN2}		100		mA
Soft-start Time	t_{SS2}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS2}		250		ohm
Conversion Effeciency (Vin=3.8V,Vout=1.1V) Iout=5A Iout=4A Iout=3A Iout=2A Iout=1 A			 68 73 78 84 89		 %

Parameter	Symbol	Min.	Typ.	Max.	Unit
Iout=500mA			90		
Iout=100 mA			81		
Iout=10 mA			79		
CH3 Buck3 Regulator (VDD_DDR)					
Input supply voltage range	V_{INPUT3}	2.7			V
Feedback Voltage, Default(Tj=25℃)	$V_{FB3(Default)}$	0.98	1.00		V
Feedback Voltage, Default(-10℃≦T_j≦+85℃)	$V_{FB3(Default)}$	0.97	1.00		V
Power Good threshold (Vout rising)	V_{PG3}		93		%
Output under voltage lockout (Vout falling)	V_{UV3}		85		%
Output over voltage lockout (Vout rising)	V_{OV3}		117		%
Load Regulation, I_{OUT3} = 100mA to 3A			1		%/A
Line Regulation, VCC3 = 3 to 5V, I_{OUT3} = 0.5A			0.1		%/V
Rated output current(If I_{CL3}=3.5A)	I_{MAX3}		3		A
Switch Current Limit (2A~3.5A programmable, step=0.5A)	I_{CL3}		3.5		A
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q3}		70		uA
Minimun Switch Current Limit (50mA~400mA programmable, step=50mA)	I_{CLMIN3}		100		mA
Soft-start Time	t_{SS3}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS3}		250		ohm
Conversion Effeciency (Vin=3.8V,Vout=1.4V)					
Iout=3A			71		%
Iout=2A			79		
Iout=1.5A			83		
Iout=1 A			87		
Iout=500mA			90		
Iout=100 mA			83		
Iout=10 mA			76		
CH4 Buck4 Regulator (VDD_IO)					
Input supply voltage range	V_{INPUT4}	2.7		5.5	V
Voltage Adjustable Range, 4bit	V_{FB4}	1.8		3.3	V
DC output voltage programmable step(gain select)			100		mV
Feedback Voltage, Default(Tj=25℃)	$V_{FB4(Default)}$	2.94	3.00	3.06	V

Parameter	Symbol	Min.	Typ.	Max.	Unit
Feedback Voltage, Default(-10℃≦T_j≦+85℃)	$V_{FB4(Default)}$	-2.91	3.00	3.09	V
Power Good threshold (Vout rising)	V_{PG4}		93		%
Output under voltage lockout (Vout falling)	V_{UV4}		85		%
Output over voltage lockout (Vout rising)	V_{OV4}		117		%
Load Regulation, I_{OUT4} = 100mA to 2.5A			1		%/A
Line Regulation, VCC4 = 3 to 5V, I_{OUT4} = 0.5A			0.1		%/V
Rated output current(If I_{CL4}=3.5A)	I_{MAX4}		2.5		A
Switch Current Limit (2A~3.5A programmable, step=0.5A)	I_{CL4}		3.5		A
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q4}		70		uA
Minimun Switch Current Limit (50mA~400mA programmable, step=50mA)	I_{CLMIN4}		100		mA
Soft-start Time	t_{SS4}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS4}		250		Ohm
Conversion Effeciency, (DCR<50mohm) Vin=3.8V,Vout=3V					%
Iout=2.5A			85		
Iout=2A			89		
Iout=1 .5A			91		
Iout=1 A			94		
Iout=500mA			95		
Iout=100mA			92		
Iout=10mA			60		
CH6 LDO1(VCC_TP)					
Input supply voltage range	V_{INPUT6}	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 4bit(step=100mv)	V_{OUT6}	1.8		3.4	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT6(Default)}$	3.234	3.300	3.366	V
V_{OUT} Output Voltage, Default(Tj= -10~85℃)	$V_{OUT6(Default)}$	3.201	3.300	3.399	V
Power Good threshold (Vout rising)	V_{PG6}		93		%
Output under voltage lockout (Vout falling)	V_{UV6}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 150mA			0.005		%/mA
V_{OUT} Line Regulation, V_{IN6} = 3 to 5V, I_{OUT6} = 0.1A			0.03		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT6}=3.3V)	PSRR6		50		dB

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output noise (10Hz to 100kHz, V_{OUT6}=3.3V)	OUT_{NOISE6}		300		uVrms
Dropout voltage @ 150mA (V_{OUT6}=3.3V)	V_{DROP6}		200		mV
Rated output current	I_{MAX6}		150		mA
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q6}		28		uA
Current Limit, VOUT6 = V_{OUT6} x 0.95	I_{CL6}	250	300		mA
Soft-start Time	t_{SS6}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS6}		400		ohm
CH7 LDO2(VCCA_33)					
Input supply voltage range	V_{INPUT7}	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 4bit(step=100mv)	V_{OUT7}	1.8		3.4	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT7(Default)}$	3.234	3.300	3.366	V
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	$V_{OUT7(Default)}$	3.201	3.300	3.399	V
Power Good threshold (Vout rising)	V_{PG7}		93		%
Output under voltage lockout (Vout falling)	V_{UV7}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 150mA			0.005		%/mA
V_{OUT} Line Regulation, V_{IN7}= 3 to 5V, I_{OUT7} = 0.1A			0.03		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT7}=3.3V)	PSRR7		50		dB
Output noise (10Hz to 100kHz, V_{OUT7}=3.3V)	OUT_{NOISE7}		300		uVrms
Dropout voltage @ 150mA (V_{OUT7}=3.3V)	V_{DROP7}		200		mV
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q7}		28		uA
Rated output current	I_{MAX7}		150		mA
Current Limit, VOUT7 = V_{OUT7} x 0.95	I_{CL7}	250	300		mA
Soft-start Time	t_{SS7}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS7}		400		Ohm
CH8 LDO3(VDD_11)					
Input supply voltage range	V_{INPUT7}	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 4bit (0.8V~2V, step=100mV, 2V~ 2.5V step=500mV)	V_{OUT8}	0.8		2.5	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT8(Default)}$	1.078	1.100	1.122	V
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	V_{OUT8} (Default)	1.067	1.100	1.133	V
Power Good threshold (Vout rising)	V_{PG8}		93		%
Output under voltage lockout (Vout falling)	V_{UV8}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 150mA			0.006		%/mA

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{OUT} Line Regulation, V_{IN8} = 3 to 5V, I_{OUT8} = 0.05A			0.015		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT8}=1.1V)	PSRR8		70		dB
Output noise (10Hz to 100kHz, V_{OUT8}=1.1V)	OUT_{NOISE8}		30		uVrms
Dropout voltage @ 100mA (V_{OUT8}=2.5V)	V_{DROP8}		200		mV
Rated output current	I_{MAX8}		100		mA
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q8}		52		uA
Current Limit, VOUT8 = V_{OUT8} x 0.95	I_{CL8}	150	200		mA
Soft-start Time	t_{SS8}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS8}		400		Ohm
CH9 LDO4(VCC_25)					
Input supply voltage range	V_{INPUT9}	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 4bit(step=100mv)	V_{OUT9}	1.8		3.4	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT9(Default)}$	2.450	2.500	2.550	V
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	$V_{OUT9(Default)}$	2.425	2.500	2.575	V
Power Good threshold (Vout rising)	V_{PG9}		93		%
Output under voltage lockout (Vout falling)	V_{UV9}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 150mA			0.005		%/mA
V_{OUT} Line Regulation, V_{IN9} = 3 to 5V, I_{OUT9} = 0.15A			0.03		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT9}=3.3V)	PSRR9		50		dB
Output noise (10Hz to 100kHz, V_{OUT9}=3.3V)	OUT_{NOISE9}		300		uVrms
Dropout voltage @ 150mA (V_{OUT9}=3.3V)	V_{DROP9}		200		mV
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q9}		28		uA
Rated output current	I_{MAX9}		150		mA
Current Limit, VOUT9 = V_{OUT9} x 0.95	I_{CL9}	250	300		mA
Soft-start Time	t_{SS9}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS9}		400		Ohm
CH10 LDO5(VCC28_CIF)					
Input supply voltage range	$V_{INPUT10}$	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 4bit(step=100mv)	V_{OUT10}	1.8		3.4	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT10(Default)}$	2.744	2.800	2.856	V
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	$V_{OUT10(Default)}$	2.716	2.800	2.884	V
Power Good threshold (Vout rising)	V_{PG10}		93		%

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output under voltage lockout (Vout falling)	V_{UV10}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 300mA			0.003		%/mA
V_{OUT} Line Regulation, V_{IN10} = 3 to 5V, I_{OUT10} = 0.3A			0.01		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT10}=3.3V)	PSRR10		52		dB
Output noise (10Hz to 100kHz, V_{OUT10}=3.3V)	$OUT_{NOISE10}$		300		uVrms
Dropout voltage @ 300mA (V_{OUT10}=2.8V)	V_{DROP10}		200		mV
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q10}		28		uA
Rated output current	I_{MAX10}		300		mA
Current Limit, VOUT10 = V_{OUT10} x 0.95	I_{CL10}	350	500		mA
Soft-start Time	t_{SS10}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS10}		400		Ohm
CH11 LDO6(VCC_12)					
Input supply voltage range	$V_{INPUT11}$	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 5bit(step=100mv)	V_{OUT11}	0.8		2.5	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT11(Default)}$	1.176	1.200	1.224	V
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	$V_{OUT11(Default)}$	1.164	1.200	1.236	V
Power Good threshold (Vout rising)	V_{PG11}		93		%
Output under voltage lockout (Vout falling)	V_{UV11}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 150mA			0.005		%/mA
V_{OUT} Line Regulation, V_{IN11} = 3 to 5V, I_{OUT11} = 0.1A			0.015		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT11}=3.3V)	PSRR11		70		dB
Output noise (10Hz to 100kHz, V_{OUT11}=3.3V)	$OUT_{NOISE11}$		30		uVrms
Dropout voltage @ 150mA (V_{OUT11}=2.5V)	V_{DROP11}		500		mV
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q11}		52		uA
Rated output current	I_{MAX11}		150		mA
Current Limit, VOUT11 = V_{OUT11} x 0.95	I_{CL11}	200	300		mA
Soft-start Time	t_{SS11}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS11}		400		Ohm
CH12 LDO7(VCC18_CIF)					
Input supply voltage rangef	$V_{INPUT12}$	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 5bit(step=100mv)	V_{OUT12}	0.8		2.5	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT12(Default)}$	1.764	1.800	1.836	V

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	$V_{OUT12(Default)}$	-1.736	1.800	1.854	V
Power Good threshold (Vout rising)	V_{PG12}		93		%
Output under voltage lockout (Vout falling)	V_{UV12}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 300mA			0.005		%/mA
V_{OUT} Line Regulation, V_{IN12} = 3 to 5V, I_{OUT12} = 0.3A			0.015		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT12}=3.3V)	PSRR12		65		dB
Output noise (10Hz to 100kHz, V_{OUT12}=3.3V)	$OUT_{NOISE12}$		50		uVrms
Dropout voltage @ 300mA (V_{OUT12}=2.5V)	V_{DROP12}		200		mV
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q12}		48		uA
Rated output current	I_{MAX12}		300		mA
Current Limit, VOUT12 = V_{OUT12} x 0.95	I_{CL12}	400	400		mA
Soft-start Time	t_{SS12}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS12}		250		Ohm
CH13 LDO8(VCC33_WIFI)					
Input supply voltage range	$V_{INPUT13}$	2.7		5.5	V
V_{OUT} Output Voltage Adjustable Range, 4bit(step=100mv)	V_{OUT13}	1.8		3.4	V
V_{OUT} Output Voltage, Default(Tj=25℃)	$V_{OUT13(Default)}$	3.234	3.300	3.366	V
V_{OUT} Output Voltage, Default(Tj=-10~85℃)	$V_{OUT13(Default)}$	3.201	3.300	3.399	V
Power Good threshold (Vout rising)	V_{PG13}		93		%
Output under voltage lockout (Vout falling)	V_{UV13}		85		%
V_{OUT} Load Regulation, I_{OUT} = 1mA to 150mA			0.003		%/mA
V_{OUT} Line Regulation, V_{IN13} = 3 to 5V, I_{OUT6} = 0.15A			0.01		%/V
Power Supply Reject Ratio (f = 10kHz, V_{OUT13}=3.3V)	PSRR13		50		dB
Output noise (10Hz to 100kHz, V_{OUT13}=3.3V)	$OUT_{NOISE13}$		300		uVrms
Dropout voltage @ 300mA (V_{OUT13}=2.8V)	V_{DROP13}		200		mV
Operating Quiescent Current, No load, V_{DD}=3.8V	I_{Q13}		30		uA
Rated output current	I_{MAX13}		300		mA
Current Limit, VOUT13 = V_{OUT13} x 0.95	I_{CL13}	400	500		mA
Soft-start Time	t_{SS13}		400		us
C_{OUT} Discharge Switch ON Resistance	R_{DIS13}		400		Ohm
CH14 SWITCH1 (VCC_SD)					
Input supply voltage range	$V_{INPUT14}$	2.7		5.5	V
Rated output current	I_{MAX14}		300		mA

Parameter	Symbol	Min.	Typ.	Max.	Unit
On resistance(Vgs=3V)			200		mohm
Current Limit	I_{CL14}	400	500		mA
C_{OUT} Discharge Switch ON Resistance	R_{DIS14}		400		Ohm
CH15 SWITCH2 (VCC_LCD)					
Input supply voltage range	$V_{INPUT15}$	2.7		5.5	V
Rated output current	I_{MAX15}		300		mA
On resistance(Vgs=3V)			200		mohm
Current Limit	I_{CL15}	400	500		mA
C_{OUT} Discharge Switch ON Resistance	R_{DIS15}		400		Ohm
Real Time Clock (RTC)					
RTC Operating Voltage Range	V_{IN}	2.5		5.5	V
RTC Supply Current	I_Q		5		uA
CLK32OUT1 jitter (open drain) (always on)		-25		+25	ns
CLK32OUT1 duty cycle		40		60	%
CLK32OUT2 jitter (open drain)		-25		+25	ns
CLK32OUT2 duty cycle		40		60	%
I2C Interface TIMING SPECIFICATIONS					
SCL clock frequency	f_{SCL}			400	kHz
SCL high time	t_{HIGH}	0.6			us
SCL low time	t_{LOW}	1.3			us
Data setup time	$t_{SU,DAT}$	0.1			us
Data hold time	$t_{HD,DAT1}$	0.1			us
Setup time for repeated start	$t_{SU,STA}$	0.1			us
HOLD time for start/repeated start	$t_{HD,STA}$	0.1			us
Rise time of SCL/SDA，C_B =400pF	t_r			300	ns
Fall width of SCL/SDA，C_B =400pF	t_f			300	ns
Pulse width of suppressed spike	t_{SP}		50		ns
Capacitive load for each of bus line	C_B			400	pF

9 STATE MACHINE DESCRIPTION

9.1 STATE MACHINE DESCRIPTION

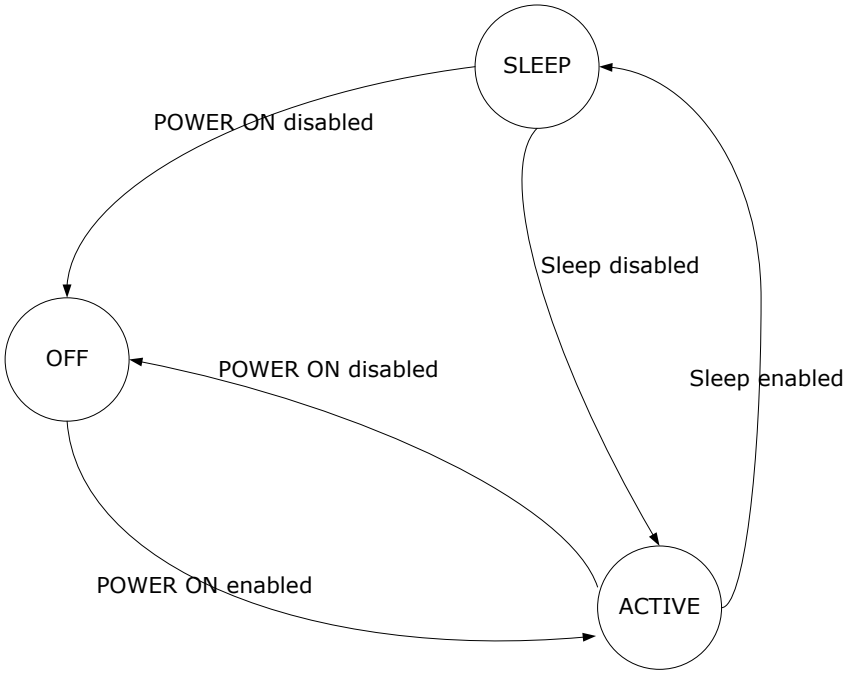


Figure 9-1 State Machine

9.2 DEVICE POWER-ON ENABLE CONDITIONS

If none of the device power-on disable conditions is met, the following conditions are available to turn on and/or maintain the ON state of the device:

- PWRON signal low level.
- Or interrupt flag active (INT low) while the device is off (NRESPWRON = 0)
  The power-on enable condition occurs only if the interrupt status bit is initially low (no previous identical interrupt pending in the status register).

The Interrupt sources expected when the device is off are:

- PWRON low-level interrupt (PWRON_INT = 1 in INT_STS_REG1 register)
- First VDC rising above plug-in threshold (PLUG_IN interrupt(PLUG_IN_INT=1 in INT_STS_REG2 register) (Charger plug in interrupt)

The Interrupt source expected if enabled when the device is off is:

- RTC Alarm interrupt (INT_ALARM_EN=1 in RTC_INT_REG and RTC_ALARM_INT = 1 in INT_STS_REG register)

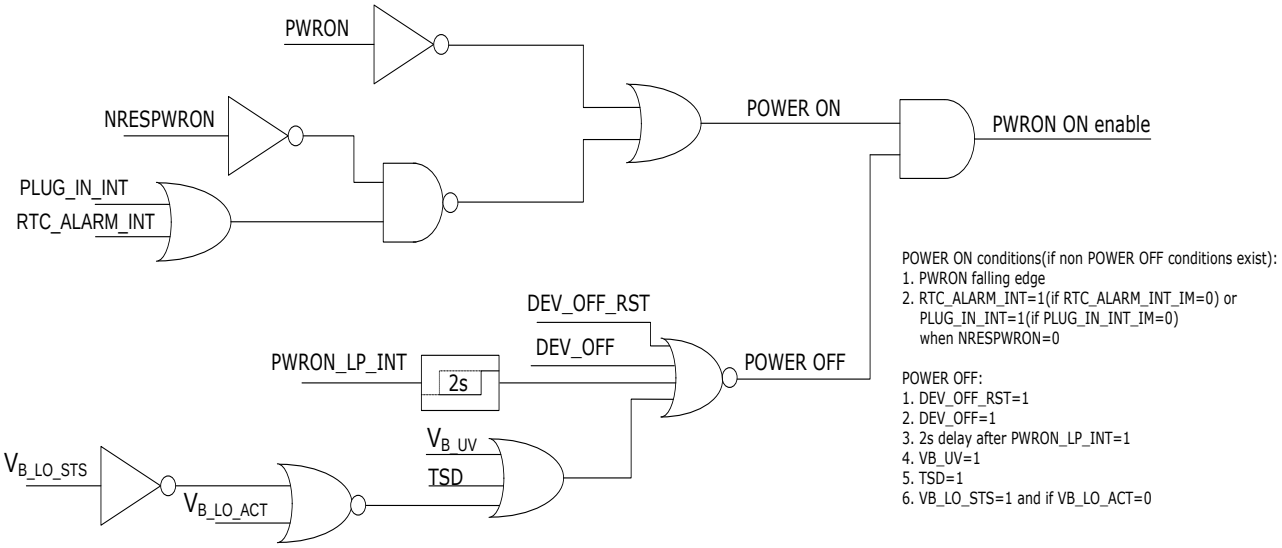


Figure 9-2 Power On Enable Control

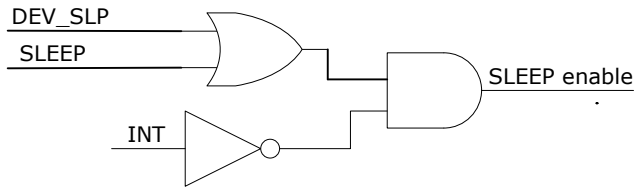
9.3 DEVICE POWER-ON DISABLE CONDITIONS

- PWRON signal low level during more than the long-press delay: $T_{DPWRONLP}$. The interrupt corresponding to this condition is PWRON_LP_INT in the INT_STS_REG register.
- Or Die temperature has reached the thermal shutdown threshold: TSD_STS=1 in THERMAL_REG).
- Or Vbat down below UVLO threshold: VB_UV_STS=1 in VB_MON_REG.
- Or DEV_OFF or DEV_OFF_RST control bit set to 1 (value of DEV_OFF is cleared when the device is in OFF state).

9.4 DEVICE SLEEP ENABLE CONDITIONS

- SLEEP signal high level.
- OR DEV_SLP control bit set to 1
- And interrupt flag inactive (INT high): No non-masked interrupt pending

The SLEEP state can be controlled by programming DEV_SLP and keeping the SLEEP state.



INT=1的条件：下面9种发生任意一种情况都会令INT=1
1. VOUT_INT=1(if VOUT_INT_IM=0)
2. VB_LO_INT=1(if VB_LO_INT_IM=0)
3. PWRON_INT=1(if PWRON_INT_IM=0)
4. PWRON_LP_INT=1(if PWRON_LP_INT_IM=0)
5. HOTDIE_INT=1(if HOTDIE_INT_IM=0)
6. RTC_ALARM_INT=1(if RTC_ALARM_INT_IM=0)
7. RTC_PERIOD_INT=1(if RTC_PERIOD_INT_IM=0)
8. PLUG_IN_INT=1(if PLUG_IN_INT_IM=0)
9. PLUG_OUT_INT=1(if PLUG_OUT_INT_IM=0)

Figure 9-3 SLEEP Enable Control

10 POWER SEQUENCE

	Power On Sequence	Preset Voltage	Power On Sequence	Preset Voltage	Power On Sequence	Preset Voltage	Power On Sequence		Preset Voltage	
Boot1, Boot0	00		01		10		11			
							B*	C*	B*	C*
BUCK1	4	1.1V/ON	4	1.2V/ON	4	1.0V/ON	2	2	1.0V/ON	1.0V/ON
BUCK2	5	1.1V/ON	5	1.2V/ON	4	1.0V/ON	3	3	1.0V/ON	1.0V/ON
BUCK3	2	X*/ON	2	X*/ON	3	X*/ON	4	4	X*/ON	X*/ON
BUCK4	1	3.0V/ON	1	3.0V/ON	1	3.0V/ON	7	6	3.3V/ON	1.8V/ON
LDO1		3.3V/OFF		3.3V/OFF	1	3.3v/ON	6	7	3.3V/ON	3.3V/ON
LDO2		3.3V/OFF	2	3.3V/ON		3.3V/OFF			1.8V/OFF	1.8V/OFF
LDO3	3	1.1V/ON	3	1.2V/ON	2	1.0V/ON	1	1	1.0V/ON	1.0V/ON
LDO4	3	2.5V/ON		2.5V/OFF	2	1.8V/ON			3.3V/OFF	3.3V/OFF
LDO5		2.8V/OFF		2.8V/OFF		2.8V/OFF	8		3.3V/ON	3.3V/OFF
LDO6		1.2V/OFF		1.2V/OFF		1.2V/OFF			1.8V/OFF	1.8V/OFF
LDO7		1.8/OFF		1.8V/OFF		1.8V/OFF	5		1.8V/ON	1.8V/OFF
LDO8		3.3V/OFF		1.8V/OFF		3.3V/OFF			3.3V/OFF	3.3V/OFF
SWITCH1	1	3.0V/ON	1	3.0V/ON	5	3.0V/ON	8		3.3V/ON	3.3V/OFF
SWITCH2		3.0V/OFF		3.0V/OFF		3.0V/OFF			1.8V/OFF	1.8V/OFF

Table 10-1 Power Start Up Sequence

The startup sequence of BOOT11 is the only difference between RK808-B and RK808-C
B*: it is RK808-B,
C*: it is RK808-C
X*: The buck3 voltage is decided by external resistors.

10.1 BOOT1=0, BOOT0 = 0

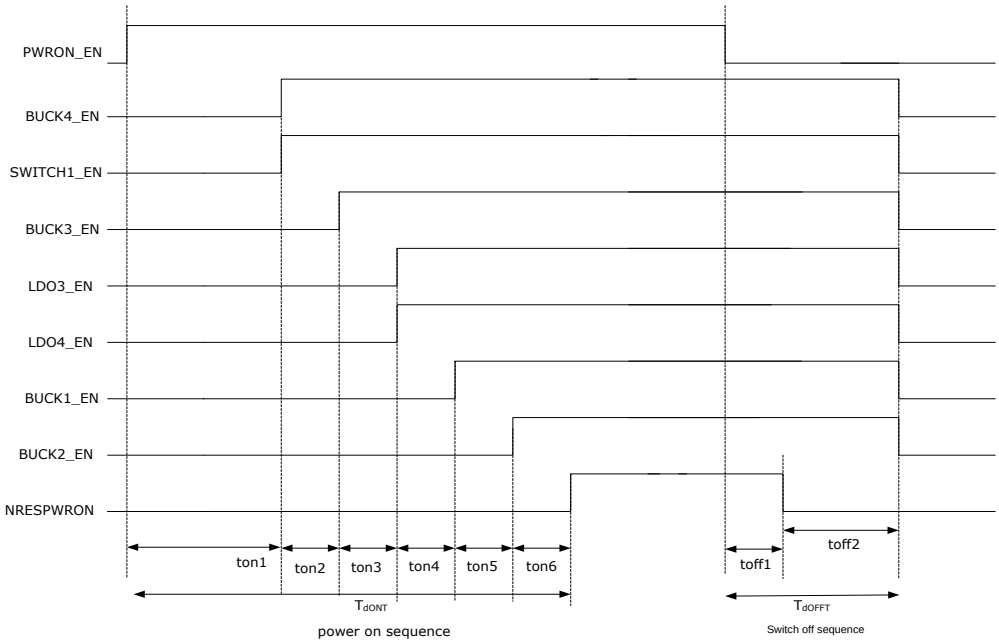


Figure 10-1 Power On/Off Timing, BOOT1=0, BOOT0=0

10.2 BOOT1=0, BOOT0 = 1

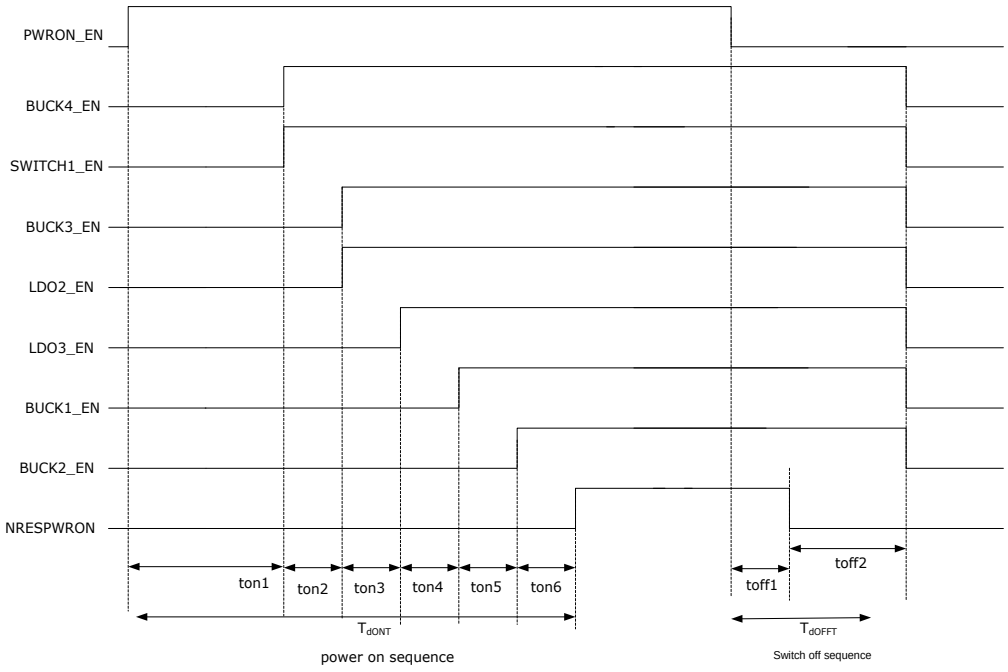


Figure 10-2 Power On/Off Timing, BOOT1=0, BOOT0=1

10.3 BOOT1=1, BOOT0 = 0

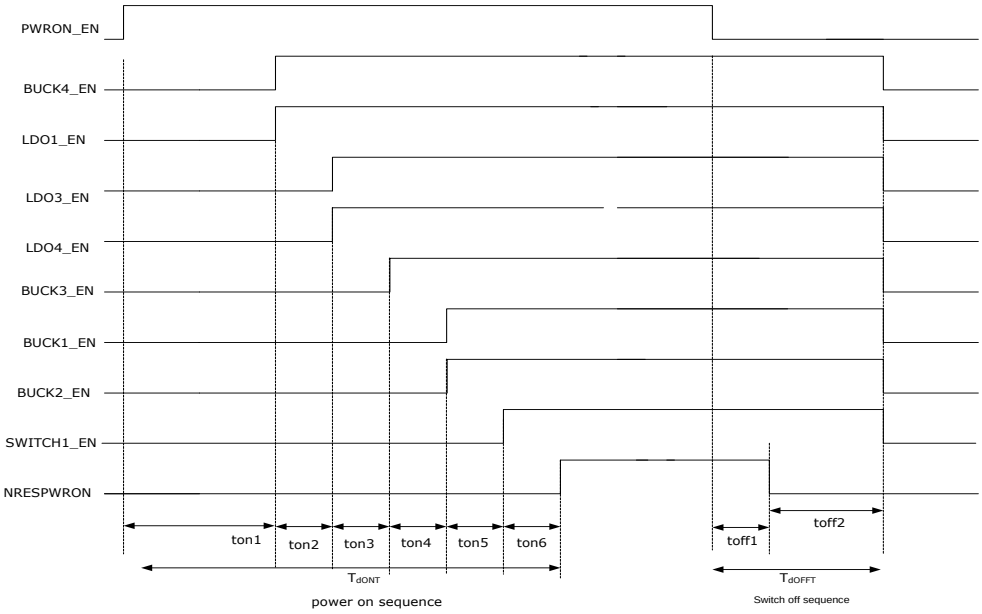
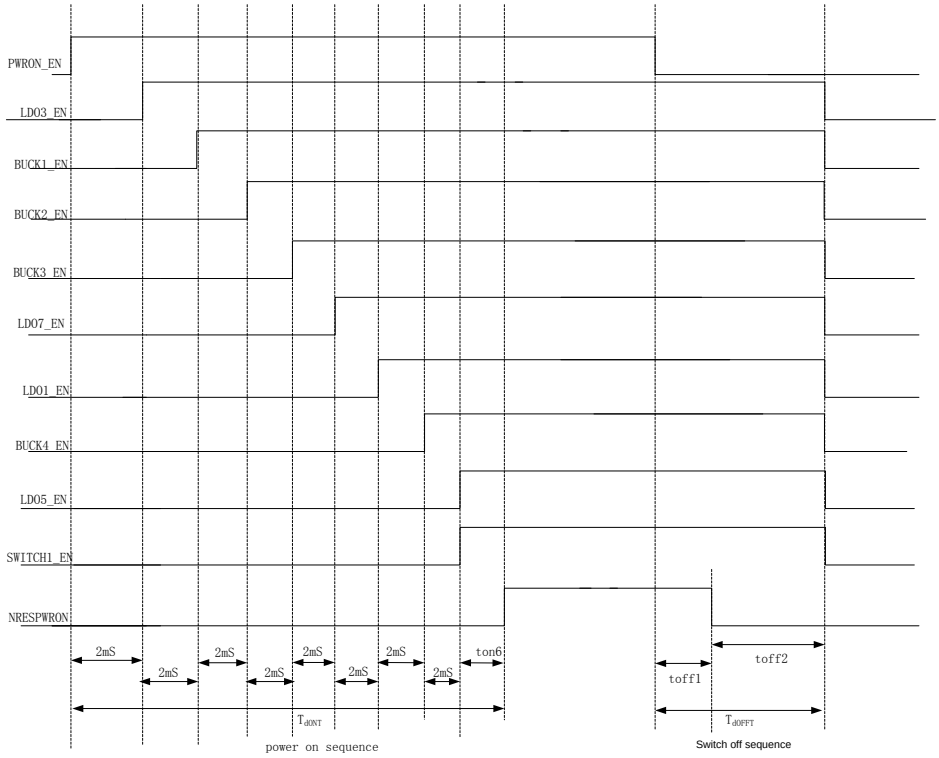


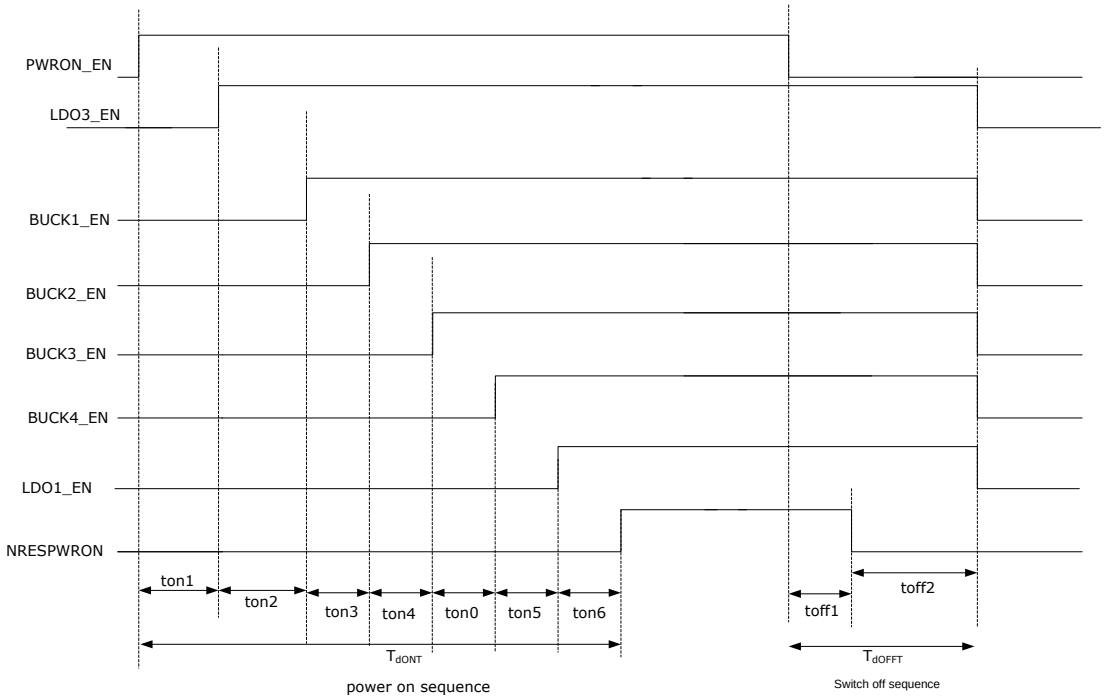
Figure 10-3 Power On/Off Timing, BOOT1=1, BOOT0=0

10.4 BOOT1=1, BOOT0 = 1(RK808-B/RK808-C)

RK808-B:



RK808-C:



10.5 BOOT TIMING CHARACTERISTIC

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNIT
ton1	Delay to 1st channel enable after power on enable debouce time		$66\times t_{CK32K}$		us
ton2	1st channel enable to 2st channel enable delay		$66\times t_{CK32K}$		us
ton3	2nd channel enable to 3rd channel enable delay		$66\times t_{CK32K}$		us
ton4	3rd channel enable to 4th channel enable delay		$66\times t_{CK32K}$		us
ton0	BUCK3 enable to BUCK4 enable delay(ONLY in BOOT11 MODE)		$132\times t_{CK32K}$		us
ton5	4th channel enable to 5th channel enable delay		$66\times t_{CK32K}$		Us
Ton6	The last channel enable to NRESPWRON rising edge delay		50		ms
toff1	PWRON disable to NRESPWRON falling delay		$1\times t_{CK32K}$		us
Toff2	NRESPWRON falling delay to supplies disable delay		2		ms

Table 10-2 Boot Timing Characteristics

11 POWER CONTROL TIMING

11.1 DEVICE TURN-ON WITH PLUG_IN

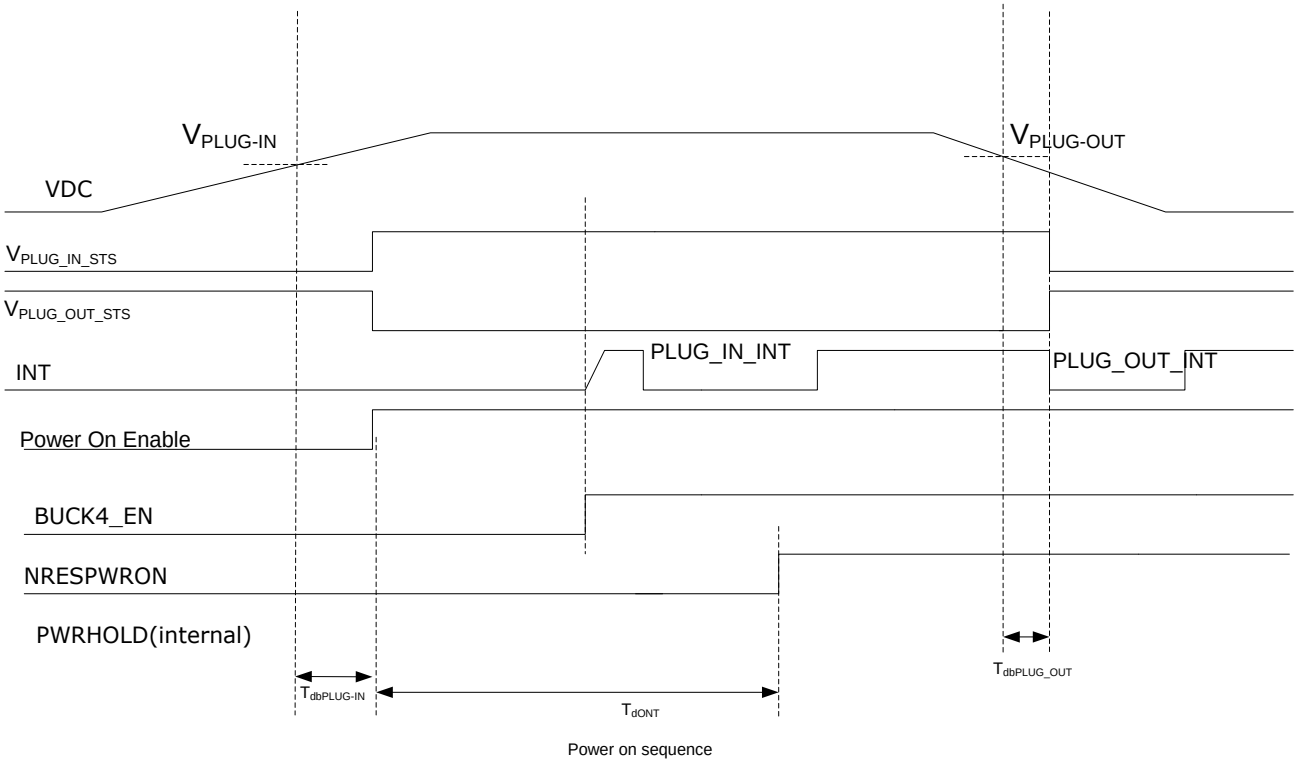


Figure 11-1Power ON Timing with VDC Plug in (PLUP_IN_INT Trigger a Power on Enable)

11.2 DEVICE TURN OFF WITH FALLING INPUT VOLTAGE

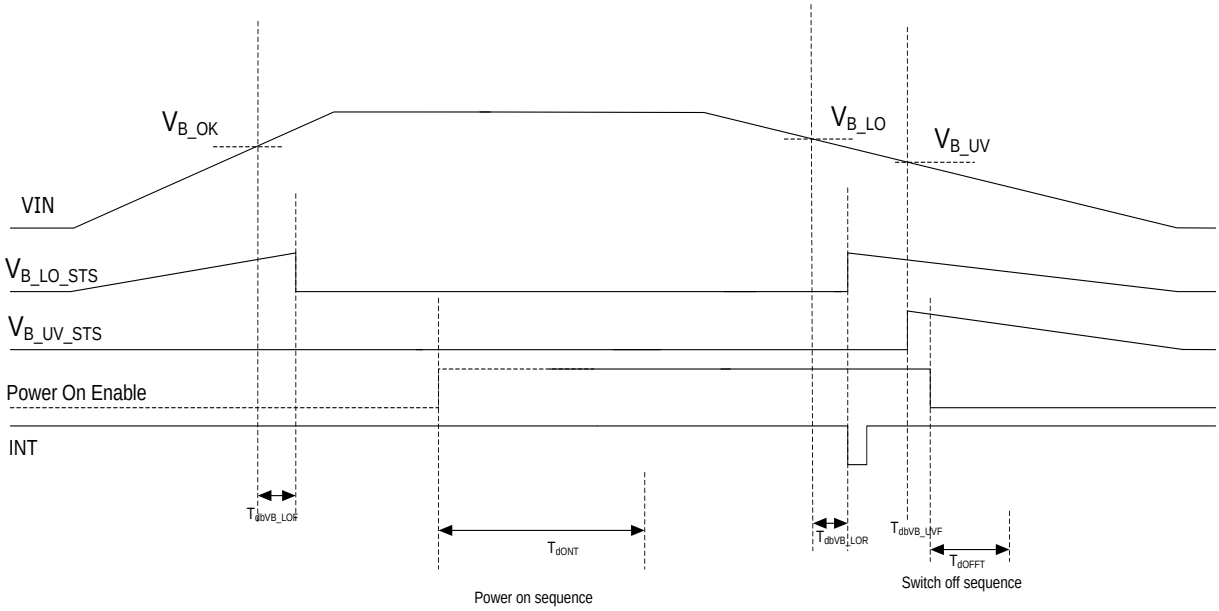


Figure 11-2 Power Control Timing with VIN Falling

11.3 TIMING CHARACTERISTICS(Vin rising/falling and Plug-in)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{dbVB_LOF}	VB_LO falling-edge debouncing delay		2		ms
T_{dONT}	Total power on delay time(ton1~ton6)		62		ms
T_{dbVB_LOR}	VB_LO rising-edge debouncing delay		2		ms
T_{dVB_UVF}	VB_UV falling-edge debouncing delay		2		ms
T_{dOFFT}	Total power off delay time		2		ms
T_{dbPLUG_IN}	VDC plug-in debouncing delay		100		ms
T_{dbPLUG_OUT}	VDC plug-out debouncing delay		100		ms

Figure 11-3 Vin and PLUG_IN Timing Characteristics

11.4 DEVICE STATE CONTROL THROUGH PWRON SIGNAL

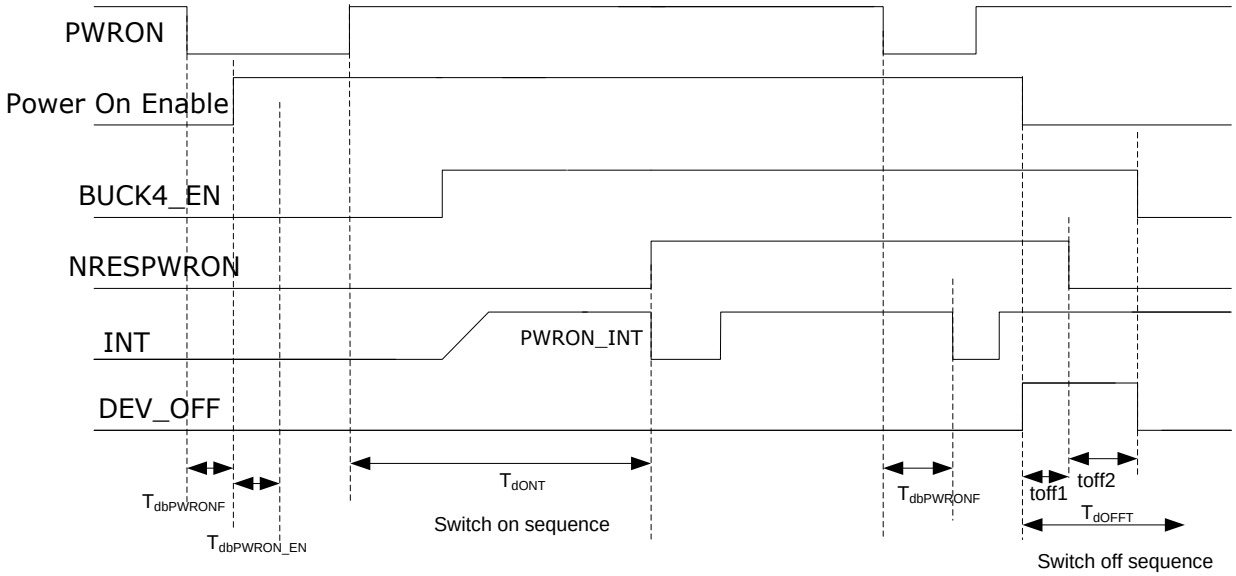


Figure 11-4 PWRON Turn-On/DEV_OFF Turn Off

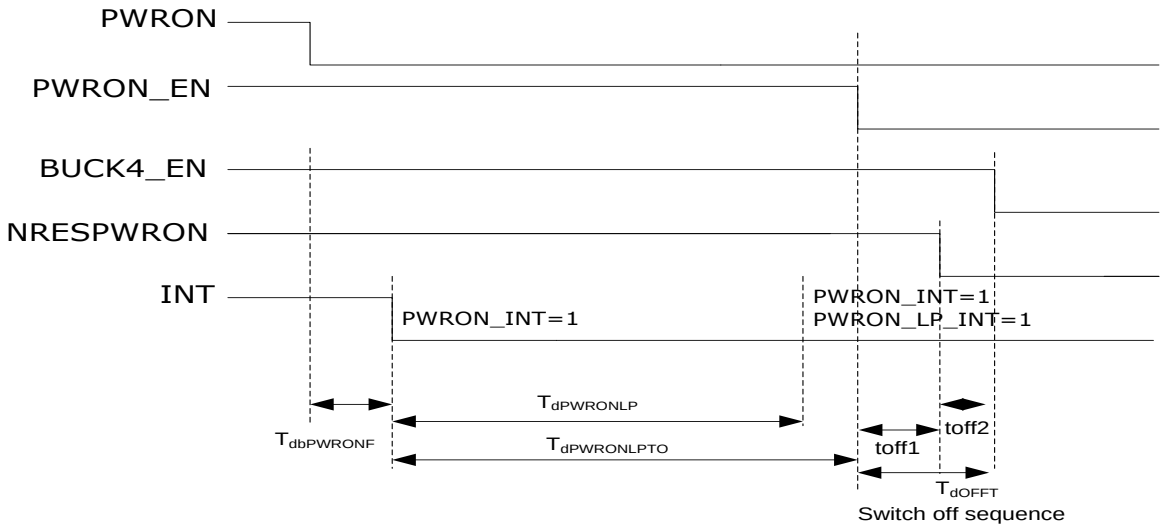


Figure 11-5 PWRON Long Press Turn Off

11.5 TIMING CHARACTERISTICS (PWRON, DEV_OFF)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$T_{dbPWRONF}$	PWRON falling-edge debouncing delay		500		ms
T_{dONT}	Total power on delay time(ton1~ton6)		62		ms
$T_{dPWRONLP}$	PWRON long press delay to interrupt (PWRON falling edge to PWRON_LP_INT=1)		6		s
$T_{dPWRONLPTO}$	PWRON long press delay to turn off (PWRON falling edge to NRESPWRON falling edge)		8		s
toff1	POWER ON disable to NRESPWRON falling delay		$1\times t_{CK32K}$		us
Toff2	NRESPWRON falling delay to supplies disable delay		2		ms
T_{dOFFT}	total power off delay time		2		ms

Table 11-1 PWRON/DEV_OFF Timing Characteristics

11.6 DEVICE SLEEP STATE CONTROL

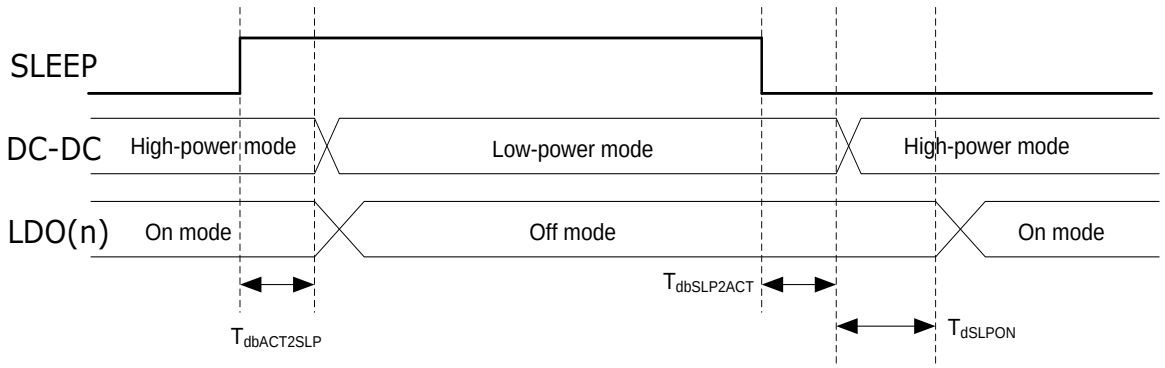


Figure 11-6 SLEEP/ACTIVE Transition Timing

11.7 TIMING CHARACTERISTICS (SLEEP)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$T_{dbACT2SLP}$	SLEEP falling-edge debouncing delay		$3\times t_{ck32k}$		us
$T_{dbSLP2ACT}$	SLEEP rising-edge debouncing delay		$3\times t_{ck32k}$		us
T_{dSLPON}	Delay to turn on enable after SLEEP rising-edge debouncing		$1\times t_{ck32k}$		us

Table 11-2 SLEEP Timing Characteristics

12 PIN ASSIGNMENT

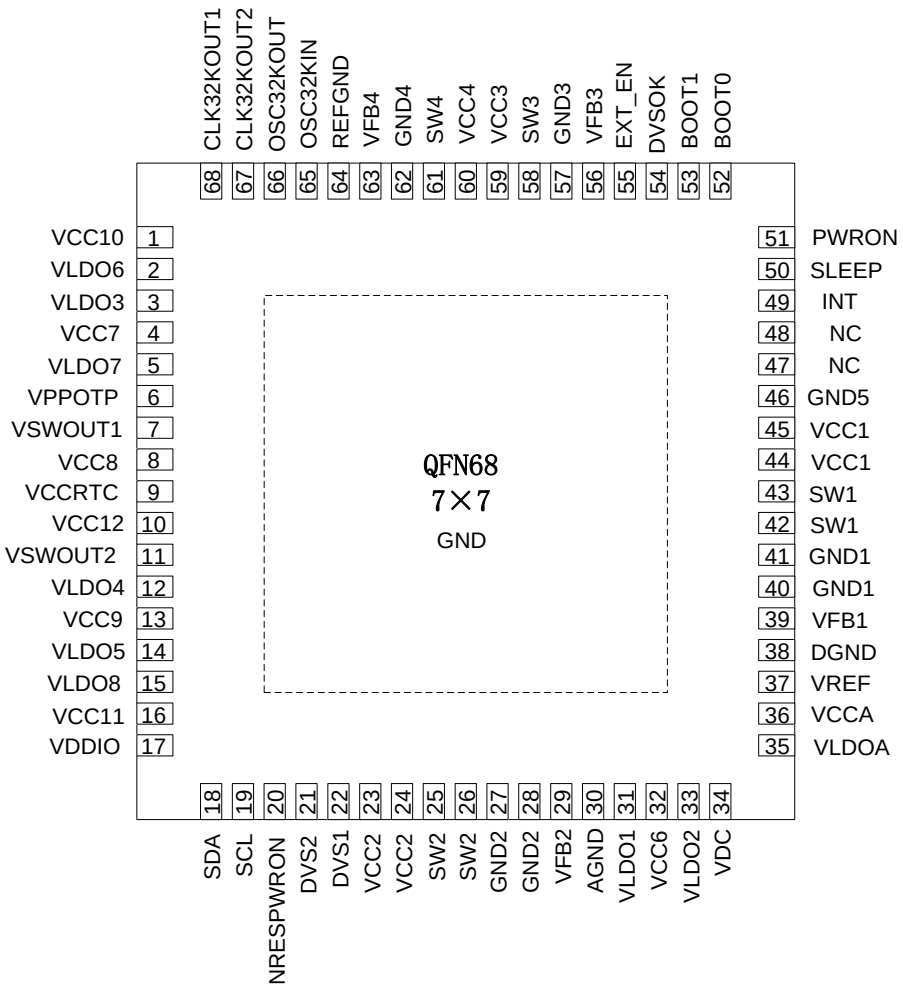


Figure 12-1 Pin Assignment

13 PINOUT DEFINITION

NO	NAME	SUPPLIES	FUNCTIONAL BLOCK	TYPE	I/O	DESCRIPTION	PU/PD
9	VCCRTC	VCCRTC /AGND	RTC	Power	O	RTC power supply	NO
65	OSC32KIN	VCCRTC /DGND		Analog	I	32KHz crystal oscillator input	NO
66	OSC32KOUT	VCCRTC /DGND		Analog	I	32KHz crystal oscillator output	NO
68	CLK32KOUT1	VCCRTC /DGND		Digital	O	32KHz clock output 1,OD output (always on)	NO
67	CLK32KOUT2	VCCRTC /DGND		Digital	O	32KHz clock output 2,OD output	PD
37	VREF	VCCA /REFGND	REFERENCE	Analog	O	bandgap voltage	PD
64	VREFGND	REFGND		Analog	Gnd	reference ground	NO
36	VCCA	VCCA /GNDA	Analog Power	Power	I	power supply for	NO
6	VPPOTP	VPPOTP /GNDA	Analog Power	Power	I	OTP power supply	NO
45	VCC1	VCC1 /GND1	BUCK1	Power	I/O	buck1 dc-dc power supply	NO
44	VCC1	VCC1 /GND1		Power	I/O	buck1 dc-dc power supply	NO
43	SW1	VCC1 /GND1		Power	I/O	buck1 dc-dc switch output	PD
42	SW1	VCC1 /GND1					
41	GND1	VCC1 /GND1		Power	Gnd	buck1 dc-dc switch ground	NO
40	GND1	VCC1 /GND1					
39	VFB1	VCC1 /REFGND		Analog	I	buck1 dc-dc switch feedback voltage	PD
23	VCC2	VCC2 /GND2	BUCK2	Power	I	buck2 dc-dc power supply	NO

24	VCC2	VCC2 /GND2		Power	I	buck2 dc-dc power supply	NO
25	SW2	VCC2 /GND2		Power	I/O	buck2 dc-dc switch output	PD
26	SW2	VCC2 /GND2		Power	I/O	buck2 dc-dc switch output	PD
27	GND2	VCC2 /GND2		Power	Gnd	buck2 dc-dc switch ground	NO
28	GND2	VCC2 /GND2		Power	Gnd	buck2 dc-dc switch ground	NO
29	VFB2	VCC2 /REFGND		Analog	I	buck2 dc-dc switch feedback voltage	PD
59	VCC3	VCC3 /GND3	BUCK3	Power	I	buck3 dc-dc power supply	NO
58	SW3	VCC3 /GND3		Power	I/O	buck3 dc-dc switch output	PD
57	GND3	VCC3 /GND3		Power	Gnd	buck3 dc-dc switch ground	NO
56	VFB3	VCC3 /REFGND		Analog	I	buck3 dc-dc switch feedback voltage	PD
60	VCC4	VCC4 /GND4	BUCK4	Power	I	buck4 dc-dc power supply	NO
61	SW4	VCC4 /GND4		Power	I/O	buck4 dc-dc switch output	PD
62	GND4	VCC4 /GND4		Power	Gnd	buck4 dc-dc switch ground	NO
63	VFB4	VCC4 /REFGND		Analog	I	buck4 dc-dc switch feedback voltage	PD
47	NC						
46	GND5	VCCA /GND5		Power	Gnd	ground	NO
48	NC						
32	VCC6	VCC6 /AGND	LDO 1~8, SWITCH1,2	Power	I	LDO1,LDO2 power supply	NO
4	VCC7	VCC7 /AGND		Power	I	LDO3,LDO7 power supply	NO
8	VCC8	VCC8 /AGND		Power	I	SWITCH1 power supply	NO

13	VCC9	VCC9 /AGND		Power	I	LDO4,LDO5 power supply	NO
1	VCC10	VCC11 /AGND		Power	I	LDO6 power supply	NO
16	VCC11	VCC11 /AGND		Power	I	LDO8 power supply	NO
10	VCC12	VCC12 /AGND		Power	I	SWITCH2 power supply	NO
31	VLDO1	VCC7 /AGND		Power	O	LDO1 regulator output	PD
33	VLDO2	VCC7 /AGND		Power	O	LDO2 regulator output	PD
3	VLDO3	VCC8 /AGND		Power	O	LDO3 regulator output	PD
12	VLDO4	VCC9 /AGND		Power	O	LDO4 regulator output	PD
14	VLDO5	VCC10 /AGND		Power	O	LDO5 regulator output	PD
2	VLDO6	VCC9 /AGND		Power	O	LDO6 regulator output	PD
5	VLDO7	VCC1 1/AGND		Power	O	LDO7 regulator output	PD
15	VLDO8	VCC11 /AGND		Power	O	LDO8 regulator output	PD
7	VSWOUT1	VCC8 /AGND		Power	O	Switch 1 output	PD
11	VSWOUT2	VCC12 /AGND		Power	O	Switch 2 output	PD
30	AGND	POWER PAD	Analog ground	Power	Gnd	Analog ground	NO
35	VLDOA	POWER PAD	LDOA	Power	I/O	supply for internal analog circuit	NO
38	DGND	POWER PAD	Digital ground	Power	Gnd	Digital ground	NO
17	VDDIO	VDDIO /DGND		Power	I/O	Digital I/O power supply	NO
50	SLEEP	VDDIO /DGND	IO	Digital	I	Active-Sleep state transition control signal	NO
20	NRESPWRON	VDDIO /DGND		Digital	O	Power off reset for AP/ External reset digital core(excludes RTC)	PD in power-off state

49	INT	VDDIO /DGND	IO	Digital	O	Interrupt flag (polarity is I2C programmable, default active high)	Programmable PU/PD
51	PWRON	VCCRTC /DGND		Digital	I	External switch-on control signal(ON button)	NO
18	SDA	VDDIO /DGND		Digital	I/O	I2C data signal	NO
19	SCL	VDDIO /DGND		Digital	I/O	I2C clock signal	NO
52	BOOT0	VCCRTC /DGND	IO	Digital	I	Power-up sequence selection	NO
53	BOOT1	VCCRTC /DGND		Digital	I	Power-up sequence selection	NO
55	EXT_EN	VCCRTC /DGND		Digital	O	Output enable for external BUCK in two-battery-cells application	PD
22	DVS1	VDDIO /DGND		Digital	I	BUCK1 DVS voltage /normal voltage transition control signal(polarity is I2C programmable, default active high)	NO
21	DVS2	VDDIO /DGND		Digital	I	BUCK2 DVS voltage /normal voltage transition control signal(polarity is I2C programmable, default active high)	NO
54	DVSOK	VDDIO /DGND		Digital	O	BUCK1 and BUCK2 power good flag after dynamic voltage setting	PD
34	VDC	VDC /AGND		Digital	I	Adapter voltage detect input	NO

14 APPLICATION NOTE

No information here.

15 REGISTER DEFINITION

15.1 REGISTER SUMMARY

HEX ADDRESS	ACTION/ DESCRIPTION	R/W	DEFAULT/ RESET
RTC REGISTERS			
00	SECONDS REG	RW	00
01	MINUTES REG	RW	50
02	HOURS REG	RW	08
03	DAYS_REG	RW	21
04	MONTHS_REG	RW	01
05	YEARS_REG	RW	13
06	WEEKS_REG	RW	01
08	ALARM_SECONDS_REG	RW	00
09	ALARM_MINUTES REG	RW	00
0A	ALARM_HOURS REG	RW	00
0B	ALARM_DAYS_REG	RW	01
0C	ALARM_MONTHS_REG	RW	01
0D	ALARM_YEARS_REG	RW	00
10	RTC_CTRL_REG	RW	00
11	RTC_STATUS_REG	RW	82
12	RTC_INT_REG	RW	00
13	RTC_COMP_LSB_REG	RW	00
14	RTC_COMP_MSB_REG	RW	00
RESERVED REGISTERS			
0E	RESERVED	RW	00
0F	RESERVED	RW	00
15	RESERVED	RW	00
16	RESERVED	RW	00
17	RESERVED	RW	00
18	RESERVED	RW	00
MISC REGISTERS			
20	CLK32KOUT_REG	RW	00

21	VB_MON_REG	RW	06
22	THERMAL_REG	RW	00
POWER CHANNEL CONTROL/MONITOR REGISTERS			
23	DCDC_EN_REG	RW	boot
24	LDO_EN_REG	RW	boot
25	SLEEP_SET_OFF_REG1	RW	00
26	SLEEP_SET_OFF_REG2	RW	00
27	DCDC_UV_STS_REG	RO	00
28	DCDC_UV_ACT_REG	RW	1F
29	LDO_UV_STS_REG	RO	00
2A	LDO_UV_ACT_REG	RW	FF
2B	DCDC_PG_REG	RO	00
2C	LDO_PG_REG	RO	00
2D	VOUT_MON_TDB_REG	RW	02
POWER CHANNEL CONFIGIGRATION REGISTERS			
2E	BUCK1_CONFIG_REG	RW	01
2F	BUCK1_ON_VSEL	RW	boot
30	BUCK1_SLP_VSEL	RW	00
31	BUCK1_DVS_VSEL	RW	00
32	BUCK2_CONFIG_REG	RW	01
33	BUCK2_ON_VSEL	RW	boot
34	BUCK2_SLP_VSEL	RW	00
35	BUCK2_DVS_VSEL	RW	00
36	BUCK3_CONFIG_REG	RW	01
37	BUCK4_CONFIG_REG	RW	00
38	BUCK4_ON_VSEL	RW	boot
39	BUCK4_SLP_VSEL_REG	RW	00
90	DCDC_ILMAX_REG	RW	00
3B	LDO1_ON_VSEL_REG	RW	boot
3C	LDO1_SLP_VSEL_REG	RW	00
3D	LDO2_ON_VSEL_REG	RW	boot
3E	LDO2_SLP_VSEL_REG	RW	00
3F	LDO3_ON_VSEL_REG	RW	boot
40	LDO3_SLP_VSEL_REG	RW	00
41	LDO4_ON_VSEL_REG	RW	boot
42	LDO4_SLP_VSEL_REG	RW	00
43	LDO5_ON_VSEL_REG	RW	boot
44	LDO5_SLP_VSEL_REG	RW	00
45	LDO6_ON_VSEL_REG	RW	boot
46	LDO6_SLP_VSEL_REG	RW	00

47	LDO7_ON_VSEL_REG	RW	boot
48	LDO7_SLP_VSEL_REG	RW	00
49	LDO8_ON_VSEL_REG	RW	boot
4A	LDO8_SLP_VSEL_REG	RW	00
4B	DEVCTRL_REG	RW	00
INTERRUPT REGISTERS			
4C	INT_STS_REG1	RW	00
4D	INT_STS_MSK_REG1	RW	00
4E	INT_STS_REG2	RW	00
4F	INT_STS_MSK_REG2	RW	00
50	IO_POL_REG	RW	06

NOTE: Address 51h through 97h are for OTP registers. Customer's accessibility to those addresses is not allowed.

15.2 REGISTER DESCRIPTION

15.2.1 RTC REGISTERS

15.2.1.1 SECONDS_REG : RTC SECOND Register

Address: 00H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	SEC1			SEC0			
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6-4	Set the second digit of the RTC seconds (0-5)
Bit 3-0	Set the first digit of the RTC seconds (0-9)
Note	BCD coding from 00 - 59

15.2.1.2 MINUTES_REG : RTC MINUTE Register

Address: 01H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	MIN1			MIN0			
Default	0	1	0	1	0	0	0	0

Description

Bit 7	Reserved

Bit 6-4 Set the second digit of the RTC minutes
Bit 3-0 Set the first digit of the RTC minutes
Note BCD coding from 00 – 59

15.2.1.3 HOURS_REG : RTC HOUR Register

Address: 02H				**Type:** RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	PM/AM	RESV	HOUR1		HOUR0			
Default	0	0	0	0	1	0	0	0

Description

Bit 7 Set PM or AM: Only used in PM-AM mode, 1: PM. 0:AM.
Bit 6 Reserved
Bit 5-4 Set the second digit of the RTC hours
Bit 3-0 Set the first digit of the RTC hours
Note HOUR1/0 BCD coding from 0-11/23

15.2.1.4 DAYS_REG : RTC DAY Register

Address: 03H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	DAY1		DAY0			
Default	0	0	1	0	0	0	0	1

Description

Bit 7-6 Reserved
Bit 5-4 Set the second digit of the RTC days
Bit 3-0 Set the first digit of the RTC days
Note BCD coding from 01 - 28/29/30/31

15.2.1.5 MONTHS_REG : RTC MONTH Register

Address: 04H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	MONTH1	MONTH0			
Default	0	0	0	0	0	0	0	1

Description

Bit 7-5 Reserved
Bit 4 Set the second digit of the RTC months
Bit 3-0 Set the first digit of the RTC months

Note BCD coding from 01 - 12

15.2.1.6 YEARS_REG : RTC YEAR Register

Address: 05H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	YEAR1				YEAR0			
Default	0	0	0	1	0	0	1	1

Description

Bit 7-5 Set the second digit of the RTC years
Bit 3-0 Set the first digit of the RTC years
Note BCD coding from 00 - 99

15.2.1.7 WEEKS_REG : RTC WEEK Register

Address: 06H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	WEEK		
Default	0	0	0	0	0	0	0	1

Description

Bit 7-3 Reserved
Bit 2-0 Set the RTC weeks
Note BCD coding from 1 - 7

15.2.1.8 ALARM_SECONDS_REG : RTC ALARM SECOND Register

Address: 08H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	ALARM_SEC1			ALARM_SEC0			
Default	0	0	0	0	0	0	0	0

Description

Bit 7 Reserved
Bit 6-4 Set the second digit of the RTC alarm seconds
Bit 3-0 Set the first digit of the RTC alarm seconds
Note BCD coding from 00 - 59

15.2.1.9 ALARM_MINUTES_REG : RTC ALARM MINUTE Register

Address: 09H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	ALARM_MIN1			ALARM_MIN0			
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6-4	Set the second digit of the RTC alarm minutes
Bit 3-0	Set the first digit of the RTC alarm minutes
Note	BCD coding from 00 - 59

15.2.1.10 ALARM_HOURS_REG : RTC ALARM HOUR Register

Address: 0AH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	ALARM_PM_AM	RESV	ALARM_HOUR1		ALARM_HOUR0			
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Set PM or AM: Only used in PM-AM mode, 1: PM. 0:AM.
Bit 6	Reserved
Bit 5-4	Set the second digit of the RTC alarm hours
Bit 3-0	Set the first digit of the RTC alarm hours
Note	HOUR1/0 BCD coding from 0-11/23

15.2.1.11 ALARM_DAYS_REG : RTC ALARM DAY Register

Address: 0BH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	ALARM_DAY1		ALARM_DAY0			
Default	0	0	0	0	0	0	0	1

Description

Bit 7-6	Reserved

Bit 5-4	Set the second digit of the RTC alarm days
Bit 3-0	Set the first digit of the RTC alarm days
Note	BCD coding from 01 - 28/29/30/31

15.2.1.12 ALARM_MONTHS_REG : RTC ALARM MONTH Register

Address: 0CH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	ALARM_MONTH1	ALARM_MONTH0			
Default	0	0	0	0	0	0	0	1

Description

Bit 7-5	Reserved
Bit 4	Set the second digit of the RTC alarm months
Bit 3-0	Set the first digit of the RTC alarm months
Note	BCD coding from 01 - 12

15.2.1.13 ALARM_YEARS_REG : RTC ALARM YEAR Register

Address: 0DH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	ALARM_YEAR1				ALARM_YEAR0			
Default	0	0	0	0	0	0	0	0

Description

Bit 7-4	Set the second digit of the RTC alarm years
Bit 3-0	Set the first digit of the RTC alarm years
Note	BCD coding from 00 - 99

15.2.1.14 RTC_CTRL_REG : RTC Control Register

Address: 10H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RTC_READSEL	GET_TIME	SET_32_COUNTER	TEST_MODE	AMPM_MODE	AUTO_COMP	ROUND_30S (Auto Clr)	STOP_RTC
Default	0	0	0	0	0	0	0	0

	Description
Bit 7	RTC_READSEL: 0: Read access directly to dynamic registers. 1: Read access to static shadowed registers
Bit 6	GET_TIME: Rising transition of this register transfers dynamic registers into static shadowed registers.
Bit 5	SET_32_COUNTER: 1: set the 32-kHz counter with COMP_REG value. It must only be used when the RTC is frozen.
Bit 4	TEST_MODE: 1: test mode (Auto compensation is enable when the 32kHz counter reaches at its end)
Bit 3	AMPM_MODE: 0: 24 hours mode. 1: 12 hours mode (PM-AM mode)
Bit 2	AUTO_COMP: 0: No auto compensation RW0. 1: Auto compensation enabled
Bit 1	ROUND_30S: 1: When 1 is written, the time is rounded to the closest minute in next second. self cleared after rounding
Bit 0	STOP_RTC: 1: RTC is frozen. 0: RTC is running. RTC_time can only be changed during RTC frozen

15.2.1.15 RTC_STATUS_REG : RTC Status Register

Address: 11H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	POWER_UP (Write 1 Clr)	ALARM (Write 1 Clr)	EVENT_1D (Write 1 Clr)	EVENT_1H (Write 1 Clr)	EVENT_1M (Write 1 Clr)	EVENT_1S (Write 1 Clr)	RUN (RO)	RESV
Default	1	0	0	0	0	0	1	0

	Description
Bit 7	POWER_UP: POWER_UP is set by a reset, is cleared by writing one in this bit.
Bit 6	ALARM: Indicates that an alarm interrupt has been generated (bit clear by writing 1) The alarm interrupt keeps its low level, until the micro-controller writes 1 in the ALARM bit of the RTC_STATUS register.The timer interrupt is a low-level pulse (15 µs duration).
Bit 5	EVENT_1D: One day has occurred
Bit 4	EVENT_1H: One hour has occurred
Bit 3	EVENT_1M: One minute has occurred
Bit 2	EVENT_1S :One secondr has occurred
Bit 1	RUN: 0, RTC is frozen. 1, RTC is running. This bit shows the real state of the RTC

Bit 0 RESEVERED

15.2.1.16 RTC_INT_REG : RTC Interrupt Register

Address: 12H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	INT_SLEEP_MASK_EN	INT_ALARM_EN	INT_TIMER_EN	EVERY	
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5	RESEVERED
Bit 4	INT_SLEEP_MASK_EN: 1: Mask periodic interrupt while the device is in SLEEP mode 0: Normal mode, no interrupt masked.
Bit 3	INT_ALARM_EN: Enable one interrupt when the alarm value is reached 1: Enable 0: Disable
Bit 2	INT_TIMER_EN:Enable periodic interrupt 1:Enable 0:Disable
Bit 1-0	EVERY: 00: every second 01: every minute 10: every hour 11: every day

15.2.1.17 RTC_COMP_LSB_REG : RTC Comensation LSB Register

Address: 13H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RTC_COMP_LSB							
Default	0	0	0	0	0	0	0	0

Description

Bit7-0	This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [LSB]

15.2.1.18 RTC_COMP_MSB_REG : RTC Compensation MSB Register

Address: 14H	Type: RW

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RTC_COMP_MSB							
Default	0	0	0	0	0	0	0	0

Description

Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [MSB]

15.2.2 MISC REGISTERS

15.2.2.1 CLK32KOUT_REG : RTC Compensation MSB Register

Address: 20H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESERVED							CLK32KOUT2_EN
Default	0	0	0	0	0	0	0	0

Description

Bit 7-1 Reserved

Bit 0 CLK32KOUT2_EN:
1. CLK32KOUT2 output is enabled
0. CLK32KOUT2 output is disabled

15.2.2.2 VB_MON_REG : Battery Voltage Monitor Register

Address: 21H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	PLUG_OUT_STS (RO)	PLUG_IN_STS (RO)	VB_UV_STS (RO)	VB_LO_ACT	VB_LO_STS (RO)	VB_LO_SEL		
Default	0	0	0	0	0	1	1	0

Description

Bit 7 PLUG_OUT_STS: charger plug-out event occurs(DC PIN voltage <3.5V)
0: no charger plug out
1: charger pluged out
This bit is read only

Bit 6 PLUG_IN_STS: charger plug-in event occurs(DC PIN voltage >3.8V)
0: no charger plug in

1: charger pluged in
This bit is read only

Bit 5 VB_UV_STS: Battery under voltage lockout status(shut down system if the bit=1)
This bit is read only

Bit 4 VB_LO_ACT: VBAT low action
0: shut down system
1: insert interrupt

Bit 3 VB_LO_STS: Battery low voltage status
0: VBAT>VB_LO_SEL
1: VBAT<VB_LO_SEL
This bit is read only

Bit 2-0 VB_LO_SEL: Battery low voltage threshold
000~111: 2.8V~ 3.5V, step=100mV

15.2.2.3 THERMAL_REG : Thermal Control Register

Address: 22H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	TSD_TEMP	HOTDIE_TEMP		HOTDIE_STS (RO)	TSD_STS (RO)
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4 TSD_TEMP: Thermal shutdown temperture threshold
0: 140℃;
1: 170℃

Bit 3-2 HOTDIE_TEMP: Hot-die temperature threshold
00: 85℃;
01: 95℃;
10: 105℃;
11: 115℃

Bit 1 HOTDIE_STS: Hot-die warning
This bit is read only bit.

Bit 0 TSD_STS: Thermal shut down

15.2.3 POWER CHANNEL CONTROL/MONITOR REGISTERS

15.2.3.1 DCDC_EN_REG : DC-DC Converter Enable Register

Address: 23H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	SWITCH2_EN	SWITCH1_EN	RESV	BUCK4_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
Default	Boot							

Description

Bit 7 Reserved

Bit 6-5 SWITCH(n): SWITCH1 and SWITCH2 enable
1, Enable
0, Disable
The default value is set by boot.

Bit 4 Reserved

Bit 3-0 BUCK(n)_EN: BUCKn enable
1, Enable
0, Disable
The default value is set by boot.

15.2.3.2 LDO_EN_REG : LDO Enable Register

Address: 24H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_EN	LDO7_EN	LDO6_EN	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN
Default	Boot							

Description

Bit 7-0 LDOn: LDO(n) enable
1, Enable
0, Disable
The default value is set by boot.

15.2.3.3 SLEEP_SET_OFF_REG1 : Sleep set Off Register #1

Address: 25H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	SWITCH2_SLP_SET_OFF	SWITCH1_SLP_SET_OFF	RESV	BUCK4_SLP_SET_OFF	BUCK3_SLP_SET_OFF	BUCK2_SLP_SET_OFF	BUCK1_SLP_SET_OFF
Default	0	0	0	0	0	0	0	0

Description

Bit 7 Reserved

Bit 6 1: Switch2 is set off in sleep mode
0: Switch2 is enable in sleep mode

Bit 5 1: Switch1 is set off in sleep mode
0: Switch1 is enable in sleep mode

Bit 4 Reserved

Bit 3 1: Buck4 is set off in sleep mode
0: Buck4 is enable in sleep mode

Bit 2 1: Buck3 is set off in sleep mode
0: Buck3 is enable in sleep mode

Bit 1 1: Buck2 is set off in sleep mode
0: Buck2 is enable in sleep mode

Bit 0 1: Buck1 is set off in sleep mode
0: Buck1 is enable in sleep mode

15.2.3.4 SLEEP_SET_OFF_REG2 : Sleep set Off Register #2

Address: 26H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_SLP_SET_OFF	LDO7_SLP_SET_OFF	LDO6_SLP_SET_OFF	LDO5_SLP_SET_OFF	LDO4_SLP_SET_OFF	LDO3_SLP_SET_OFF	LDO2_SLP_SET_OFF	LDO1_SLP_SET_OFF
Default	0	0	0	0	0	0	0	0

Description

Bit 7 1: LDO8 is set off in sleep mode
0: LDO8 is enable in sleep mode

Bit 6 1: LDO7 is set off in sleep mode
0: LDO7 is enable in sleep mode

Bit 5 1: LDO6 is set off in sleep mode
0: LDO6 is enable in sleep mode

Bit 4	1: LDO5 is set off in sleep mode 0: LDO5 is enable in sleep mode
Bit 3	1: LDO4 is set off in sleep mode 0: LDO4 is enable in sleep mode
Bit 2	1: LDO3 is set off in sleep mode 0: LDO3 is enable in sleep mode
Bit 1	1: LDO2 is set off in sleep mode 0: LDO2 is enable in sleep mode
Bit 0	1: LDO1 is set off in sleep mode 0: LDO1 is enable in sleep mode

15.2.3.5 DCDC_UV_STS_REG : DC-DC Under Voltage Status Register

Address: 27H				Type: R				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	BUCK4_UV_STS	BUCK3_UV_STS	BUCK2_UV_STS	BUCK1_UV_STS
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5	Reserved
Bit 4	Reserved
Bit 3	BUCK4_UV_STS: BUCK4 under voltage flag. 1: Output voltage drop below 85% of nominal voltage 0: Normal
Bit 2	BUCK3_UV_STS: BUCK3 under voltage flag. 1: Output voltage drop below 85% of nominal voltage 0: Normal
Bit 1	BUCK2_UV_STS: BUCK2 under voltage flag. 1: Output voltage drop below 85% of nominal voltage 0: Normal
Bit 0	BUCK1_UV_STS: BUCK1 under voltage flag. 1: Output voltage drop below 85% of nominal voltage 0: Normal

15.2.3.6 DCDC_UV_ACT_REG : DC-DC Under Voltage Action Register

Address: 28H				Type: R				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

SYMBOL	RESV	RESV	RESV	RESV	BUCK4_UV_ACT	BUCK3_UV_ACT	BUCK2_UV_ACT	BUCK1_UV_ACT
Default	0	0	0	1	1	1	1	1

Description

Bit 7-5 Reserved

Bit 4 Reserved

Bit 3 BUCK4_UV_ACT: BUCK4 under voltage flag.
1: restart converter
0: No effect

Bit 2 BUCK3_UV_ACT: BUCK3 under voltage flag.
1: restart converter
0: No effect

Bit 1 BUCK2_UV_ACT: BUCK2 under voltage flag.
1: restart converter
0: No effect

Bit 0 BUCK1_UV_ACT: BUCK1 under voltage flag.
1: restart converter
0: No effect

15.2.3.7 LDO_UV_STS_REG : LDO Under Voltage Status Register

Address: 29H				Type: R				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_UV_STS	LDO7_UV_STS	LDO6_UV_STS	LDO5_UV_STS	LDO4_UV_STS	LDO3_UV_STS	LDO2_UV_STS	LDO1_UV_STS
Default	0	0	0	0	0	0	0	0

Description

Bit 7 LDO8_UV_STS: LDO8 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 6 LDO7_UV_STS: LDO7 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 5 LDO6_UV_STS: LDO6 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 4 LDO5_UV_STS: LDO5 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 3 LDO4_UV_STS: LDO4 under voltage flag.

1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 2 LDO3_UV_STS: LDO3 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 1 LDO2_UV_STS: LDO2 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

Bit 0 LDO1_UV_STS: LDO1 under voltage flag.
1, Output voltage drop below 85% of nominal voltage
0, Normal

15.2.3.8 LDO_UV_ACT_REG : LDO Under Voltage Action Register

Address: 2AH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_UV_ACT	LDO7_UV_ACT	LDO6_UV_ACT	LDO5_UV_ACT	LDO4_UV_ACT	LDO3_UV_ACT	LDO2_UV_ACT	LDO1_UV_ACT
Default	1	1	1	1	1	1	1	1

Description

Bit 7 LDO8_UV_ACT: LDO8 under voltage action
1: restart converter
0: No effect

Bit 6 LDO7_UV_ACT: LDO7 under voltage action
1: restart converter
0: No effect

Bit 5 LDO6_UV_ACT: LDO6 under voltage action
1: restart converter
0: No effect

Bit 4 LDO5_UV_ACT: LDO5 under voltage action
1: restart converter
0: No effect

Bit 3 LDO4_UV_ACT: LDO4 under voltage action
1: restart converter
0: No effect

Bit 2 LDO3_UV_ACT: LDO3 under voltage action
1: restart converter
0: No effect

Bit 1 LDO2_UV_ACT: LDO2 under voltage action
1: restart converter

0: No effect

Bit 0 LDO1_UV_ACT: LDO1 under voltage action
1: restart converter
0: No effect

15.2.3.9 DCDC_PG_REG : DC-DC Converter Power Good Status Register

Address: 2BH				Type: R				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	BUCK4_PG_STS	BUCK3_PG_STS	BUCK2_PG_STS	BUCK1_PG_STS
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4 Reserved

Bit 3 BUCK4_PG_STS : BUCK4 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage

Bit 2 BUCK3_PG_STS : BUCK3 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage

Bit 1 BUCK2_PG_STS : BUCK2 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage

Bit 0 BUCK1_PG_STS : BUCK1 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage

15.2.3.10 LDO_PG_REG : LDO Power Good Status Register

Address: 2CH				Type: R				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_PG_STS	LDO7_PG_STS	LDO6_PG_STS	LDO5_PG_STS	LDO4_PG_STS	LDO3_PG_STS	LDO2_PG_STS	LDO1_PG_STS
Default	0	0	0	0	0	0	0	0

Description	
Bit 7	LDO8_PG_STS : LDO8 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 6	LDO7_PG_STS : LDO7 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 5	LDO6_PG_STS : LDO6 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 4	LDO5_PG_STS : LDO5 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 3	LDO4_PG_STS : LDO4 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 2	LDO3_PG_STS : LDO3 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 1	LDO2_PG_STS : LDO2 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage
Bit 0	LDO1_PG_STS : LDO1 power good flag. 1: Power good, Vout>90% of setting voltage 0: Power not good, Vout<90% of setting voltage

15.2.3.11 VOUT_MON_TDB_REG : VOUT Debounce Monitor Register

Address: 2DH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	RESV	VOUT_MON_TDB	
Default	0	0	0	0	0	0	1	0

Description	
Bit 7-2	Reserved
Bit 1-0	VOUT_MON_TDB: Vout monitor debouncing time(UV_STS rising edge and PG_STS rising edge debounce time) 00: 62us 01: 124us

10: 186us(default)
11: 248us

15.2.4 POWER CHANNEL CONFIGURATION REGISTERS

15.2.4.1 BUCK1_CONFIG_REG : BUCK1 Configuration Register

Address: 2EH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	BUCK1_PHASE	RESV	BUCK1_RATE		BUCK1_ILMIN		
Default	0	0	0	0	0	0	0	1

Description

Bit 7 Reserved

Bit 6 BUCK1_PHASE,
0: Normal,
1: Inverted

Bit 5 Reserved

Bit 4-3 BUCK1_RATE: Voltage change rate after DVS
00: 2mv/us
01: 4mv/us
10: 6mv/us
11: 10mv/us

Bit 2-0 BUCK1_ILMIN: The minimum of inductor current
000: 50mA
001: 100mA(default);
010: 150mA
011: 200mA
100: 250mA
101: 300mA
110: 350mA
111: 400mA

15.2.4.2 BUCK1_ON_VSEL : BUCK1 Active Mode Register

Address: 2FH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	BUCK1_ON_VSEL					

Default	Boot

Description

Bit 7	Reserved
Bit 6	Reserved
Bit 5-0	BUCK1_ON_VSEL: BUCK1 active mode voltage select, 0.7125V~1.5V ,step=12.5mV 000 000: 0.7125V 000 001: 0.725V …… 111 111: 1.5V The default value is set by boot.

15.2.4.3 BUCK1_SLP_VSEL : BUCK1 Sleep Mode Register

Address: 30H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	BUCK1_SLP_VSEL					
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6	Reserved
Bit 5-0	BUCK1_SLP_VSEL: BUCK1 sleep mode voltage select, 0.7125V~1.5V ,step=12.5mV 000 000: 0.7125V 000 001: 0.725V …… 111 111: 1.5V

15.2.4.4 BUCK1_DVS_VSEL : BUCK1 DVS Mode Register

Address: 31H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	BUCK1_DVS_VSEL					
Default	0	0	0	0	0	0	0	0

Description

Bit 7-6	Reserved
Bit 5-0	BUCK1_DVS_VSEL: BUCK1 DVS voltage select, 0.7125V~1.5V ,step=12.5mV 000 000: 0.7125V 000 001: 0.725V …… 111 111: 1. 5V

15.2.4.5 BUCK2_CONFIG_REG : BUCK2 Configuration Register

Address: 32H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	BUCK2_ PHASE	RESV	BUCK2_RATE		BUCK2_ILMIN		
Default	0	0	0	0	0	0	0	1

Description

Bit 7	Reserved
Bit 6	BUCK2_PHASE, 0: Normal, 1: Inverted
Bit 5	Reserved
Bit 4-3	BUCK2_RATE: Voltage change rate after DVS 00: 2mv/us 01: 4mv/us 10: 6mv/us 11: 10mv/us
Bit 2-0	BUCK2_ILMIN: The minimum of inductor current 000: 50mA 001: 100mA(default); 010: 150mA 011: 200mA 100: 250mA 101: 300mA 110: 350mA 111: 400mA

15.2.4.6 BUCK2_ON_VSEL : BUCK2 Active Mode Register

Address: 33H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	BUCK2_ON_VSEL					
Default	Boot							

Description

Bit 7	Reserved
Bit 6	Reserved
Bit 5-0	BUCK2_ON_VSEL: BUCK2 active mode voltage select, 0.7125V~1.5V ,step=12.5mV 000 000: 0.7125V 000 001: 0.725V …… 111 111: 1.5V The default value is set by boot.

15.2.4.7 BUCK2_SLP_VSEL : BUCK2 Sleep Mode Register

Address: 34H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	BUCK2_SLP_VSEL					
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6	Reserved
Bit 5-0	BUCK2_SLP_VSEL: BUCK1 sleep mode voltage select, 0.7125V~1.5V ,step=12.5mV 000 000: 0.7125V 000 001: 0.725V …… 111 111: 1.5V

15.2.4.8 BUCK2_DVS_VSEL : BUCK2 DVS Mode Register

Address: 35H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	BUCK2_DVS_VSEL					
Default	0	0	0	0	0	0	0	0

Description

Bit 7-6 Reserved

Bit 5-0 BUCK2_DVS_VSEL: BUCK1 DVS voltage select,
0.7125V~1.5V ,step=12.5mV
000 000: 0.7125V
000 001: 0.725V
……
111 111: 1.5V

15.2.4.9 BUCK3_CONFIG_REG : BUCK3 Configuration Register

Address: 36H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	BUCK3_PHASE	RESV	RESV	RESV	BUCK3_ILMIN		
Default	0	0	0	0	0	0	0	1

Description

Bit 7 Reserved

Bit 6 BUCK3_PHASE,
0: Normal,
1: Inverted

Bit 5-3 Reserved

Bit 2-0 BUCK3_ILMIN: The minimum of inductor current
000: 50mA
001: 100mA(default);
010: 150mA
011: 200mA
100: 250mA
101: 300mA
110: 350mA
111: 400mA

15.2.4.10 BUCK4_CONFIG_REG : BUCK4 Configuration Register

Address: 37H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	BUCK4_PHASE	RESV	RESV	RESV	BUCK4_ILMIN		
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6	BUCK4_PHASE, 0: Normal, 1: Inverted
Bit 2-0	BUCK4_ILMIN:The minimum of inductor current 000: 50mA 001: 100mA(default); 010: 150mA 011: 200mA 100: 250mA 101: 300mA 110: 350mA 111: 400mA

15.2.4.11 BUCK4_ON_VSEL : BUCK4 Active Mode Register

Address: 38H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	BUCK4_ON_VSEL			
Default	Boot							

Description

Bit 7	Reserved
Bit 6-4	Reserved
Bit 3-0	BUCK4_ON_VSEL: BUCK4 active mode voltage select, 1.8V~3.3V ,step=100mV 0000: 1.8V 0001: 1.9V …… 1110: 3.2V 1111: 3.3V

the default value is set by boot.

15.2.4.12 BUCK4_SLP_VSEL : BUCK4 Sleep Mode Register

Address: 39H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	BUCK4_SLP_VSEL			
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6-4	Reserved
Bit 3-0	BUCK4_SLP_VSEL: BUCK4 sleep mode voltage select, 1.8V~3.3V ,step=100mV 0000: 1.8V 0001: 1.9V …… 1110: 3.2V 1111: 3.3V

15.2.4.13 LDO1_ON_VSEL_REG : LDO1 Active Mode Voltage Select

Address: 3BH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO1_ON_VSEL				
Default	Boot							

Description

Bit 7-5	Reserved
Bit 4-0	LDO1_ON_VSEL: LDO1 active mode voltage select. 1.8V~3.4V, step=0.1V 00000: 1.8V 00001: 1.9V ….

01110: 3.2V
01111: 3.3V
10000: 3.4V
the default value is set by boot.

15.2.4.14 LDO1_SLP_VSEL_REG : LDO1 Sleep Mode Voltage Select

Address: 3CH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO1_SLP_VSEL				
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved
Bit 4-0 LDO1_SLP_VSEL: LDO1 SLEEP mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V

15.2.4.15 LDO2_ON_VSEL_REG : LDO2 Active Mode Voltage Select

Address: 3DH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO2_ON_VSEL				
Default	Boot							

Description

Bit 7-5 Reserved
Bit 4-0 LDO2_ON_VSEL: LDO2 active mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V

10000: 3.4V
the default value is set by boot.

15.2.4.16 LDO2_SLP_VSEL_REG : LDO2 Sleep Mode Voltage Select

Address: 3EH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO2_SLP_VSEL				
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4-0 LDO2_SLP_VSEL: LDO2 SLEEP mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V

15.2.4.17 LDO3_ON_VSEL_REG : LDO3 Active Mode Voltage Sel

Address: 3FH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	LDO3_ON_VSEL			
Default	Boot							

Description

Bit 7-4 Reserved

Bit 3-0 LDO3_ON_VSEL: LDO3 active voltage select.
0.8V~2.5V, step=0.1V
0000: 0.8V
0001: 0.9V
….
1100: 2.0V
1101: 2.2V
1111: 2.5V
the default value is set by boot.

15.2.4.18 LDO3_SLP_VSEL_REG : LDO3 Sleep Mode Voltage Select

Address: 40H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	LDO3_SLP_VSEL			
Default	0	0	0	0	0	0	0	0

Description

Bit 7-4 Reserved

Bit 3-0 LDO3_SLP_VSEL: LDO3 SLEEP mode voltage select.
0.8V~2.5V, step=0.1V
0000: 0.8V
0001: 0.9V
….
1100: 2.0V
1101: 2.2V
1111: 2.5V
the default value is set by boot.

15.2.4.19 LDO4_ON_VSEL_REG : LDO4 Active Mode Voltage Select

Address: 41H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO4_ON_VSEL				
Default	Boot							

Description

Bit 7-5 Reserved

Bit 4-0 LDO4_ON_VSEL: LDO4 active mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V
the default value is set by boot.

15.2.4.20 LDO4_SLP_VSEL_REG : LDO4 Sleep Mode Voltage Select

Address: 42H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO4_SLP_VSEL				
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4-0 LDO2_SLP_VSEL: LDO2 SLEEP mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V

15.2.4.21 LDO5_ON_VSEL_REG : LDO5 Active Mode Voltage Select

Address: 43H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO5_ON_VSEL				
Default	Boot							

Description

Bit 7-5 Reserved

Bit 4-0 LDO5_ON_VSEL: LDO5 active mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V
the default value is set by boot.

15.2.4.22 LDO5_SLP_VSEL_REG : LDO5 Sleep Mode Voltage Select

Address: 44H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO5_SLP_VSEL				
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4-0 LDO5_SLP_VSEL: LDO5 SLEEP mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V

15.2.4.23 LDO6_ON_VSEL_REG : LDO6 Active Mode Voltage Select

Address: 45H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO6_ON_VSEL				
Default	Boot							

Description

Bit 7-5 Reserved

Bit 4-0 LDO6_ON_VSEL: LDO6 active mode voltage select.
0.8V~2.5V, step=0.1V
00000: 0.8V
00001: 0.9V
……
10000: 2.4V
10001: 2.5V
the default value is set by boot.

15.2.4.24 LDO6_SLP_VSEL_REG : LDO6 Sleep Mode Voltage Select

Address: 46H	Type: RW

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO6_SLP_VSEL				
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4-0 LDO6_SLP_VSEL: LDO6 SLEEP mode voltage select.
0.8V~2.5V, step=0.1V
00000: 0.8V
00001: 0.9V
……
10000: 2.4V
10001: 2.5V

15.2.4.25 LDO7_ON_VSEL_REG : LDO7 Active Mode Voltage Select

Address: 47H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO7_ON_VSEL				
Default	Boot							

Description

Bit 7-5 Reserved

Bit 4-0 LDO7_ON_VSEL: LDO7 active mode voltage select.
0.8V~2.5V, step=0.1V
00000: 0.8V
00001: 0.9V
……
10000: 2.4V
10001: 2.5V
the default value is set by boot.

15.2.4.26 LDO7_SLP_VSEL_REG : LDO7 Sleep Mode Voltage Select

Address: 48H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

SYMBOL	RESV	RESV	RESV	LDO7_SLP_VSEL				
Default	0	0	0	0	0	0	0	0

Description

Bit 7-5	Reserved
Bit 4-0	LDO7_SLP_VSEL: LDO7 SLEEP mode voltage select. 0.8V~2.5V, step=0.1V 00000: 0.8V 00001: 0.9V …… 10000: 2.4V 10001: 2.5V

15.2.4.27 LDO8_ON_VSEL_REG : LDO8 Active Mode Voltage Select

Address: 49H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO8_ON_VSEL				
Default	Boot							

Description

Bit 7-5	Reserved
Bit 4-0	LDO8_ON_VSEL: LDO8 active mode voltage select. 1.8V~3.4V, step=0.1V 00000: 1.8V 00001: 1.9V …. 01110: 3.2V 01111: 3.3V 10000: 3.4V the default value is set by boot.

15.2.4.28 LDO8_SLP_VSEL_REG : LDO8 Sleep Mode Voltage Select

Address: 4AH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO8_SLP_VSEL				

Default	0	0	0	0	0	0	0	0

Description

Bit 7-5 Reserved

Bit 4-0 LDO8_SLP_VSEL: LDO8 SLEEP mode voltage select.
1.8V~3.4V, step=0.1V
00000: 1.8V
00001: 1.9V
….
01110: 3.2V
01111: 3.3V
10000: 3.4V

15.2.4.29 DEVCTRL_REG : Device Control Register

Address: 4BH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	PWRON_LP_OFF_TIME		DEV_OFF_RST	RESV	DEV_SLP	DEV_OFF
Default	0	0	0	0	0	0	0	0

Description

Bit 7-6 Reserved

Bit 5-4 PWRON_LP_OFF_TIME: PWRON long press turn off time:
00: 6s
01: 8s
10: 10s
11: 12s

Bit 3 DEV_OFF_RST: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event) and activate reset of the digital core.

Bit 2 Reserved

Bit 1 DEV_SLP: Write 1 allows SLEEP device state (if DEV_OFF = 0 and DEV_OFF_RST = 0).
Write '0' will start a SLEEP to ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_OFF_RST = 0). This bit is cleared in OFF state.

Bit 0 DEV_OFF: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state.

15.2.5 INTERRUPT REGISTERS

15.2.5.1 INT_STS_REG1 : Interrupt Status Register #1

Address: 4CH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RTC_PERIOD_INT (Write 1 Clr)	RTC_ALARM_INT (Write 1 Clr)	HOTDIE_INT (Write 1 Clr)	PWRON_LP_INT (Write 1 Clr)	PWRON_INT (Write 1 Clr)	VB_LO_INT (Write 1 Clr)	VOUT_LO_INT (Write 1 Clr)
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6	RTC_PERIOD_INT: RTC period event interrupt.
Bit 5	RTC_ALARM_INT: RTC alarm event interrupt.
Bit 4	HOTDIE_INT: Hot die event interrupt status.
Bit 3	PWRON_LP_INT: PWRON PIN long press event interrupt status.
Bit 2	PWRON_INT: PWRON event interrupt status.
Bit 1	VB_LO_INT: Battery under voltage alarm event interrupt status.
Bit 0	VOUT_LO_INT: VOUT under voltage alarm event interrupt status
Note:	1: Interrupt asserted, write "1" to clear
	0: No interrupt

15.2.5.2 INT_MSK_REG1 : Interrupt Mask Register #1

Address: 4DH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RTC_PERIOD_IM	RTC_ALARM_IM	HOTDIE_IM	PWRON_LP_IM	PWRON_IM	VB_LO_IM	VOUT_LO_IM
Default	0	0	0	0	0	0	0	0

Description

Bit 7	Reserved
Bit 6	RTC_PERIOD_INT: RTC period event interrupt mask.
Bit 5	RTC_ALARM_INT: RTC alarm event interrupt mask.
Bit 4	HOTDIE_INT: Hot die event interrupt status mask.
Bit 3	PWRON_LP_INT: PWRON PIN long press event interrupt status mask.
Bit 2	PWRON_INT: PWRON event interrupt status mask.
Bit 1	VB_LO_INT: Battery under voltage alarm event interrupt status mask.

Bit 0 VOUT_LO_IM: Vout under voltage alarm event interrupt status mask

Note: 1: Mask the specified interrupt
0: Do not mask the specified interrupt

15.2.5.3 INT_STS_REG2 : Interrupt Status Register #2

Address: 4EH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	RESV	PLUG_OUT_INT (Write 1 Clr)	PLUG_IN_INT (Write 1 Clr)
Default	0	0	0	0	0	0	0	0

Description

Bit 7-2 Reserved

Bit 1 PLUG_OUT_INT: charger plug out event interrupt(PLUG_IN_STS falling edge interrupt)

Bit 0 PLUG_IN_INT: charger plug in event interrupt(PLUG_IN_STS rising edge interrupt)

Note: Write "1" to clear.

15.2.5.4 INT_STS_MSK_REG2 : Interrupt Status Register #2

Address: 4FH				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	RESV	PLUG_OUT_INT_IM	PLUG_IN_INT_IM
Default	0	0	0	0	0	0	0	0

Description

Bit 7-2 Reserved

Bit 1 PLUG_OUT_INT_IM: Charger plug out event interrupt mask.
1: Mask the interrupt
0: Do not mask the interrupt

Bit 0 PLUG_IN_INT_IM: Charger plug in event interrupt mask
1: Mask the interrupt
0: Do not mask the interrupt

15.2.5.5 IO_POL_REG : IO Polarity Register

Address: 50H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	DVS2_POL	DVS1_POL	INT_POL
Default	0	0	0	0	0	1	1	0

Description

Bit 7-3 Reserved

Bit 2 DVS2_POL: DVS2 pin polarity
0: active low
1: active high

Bit 1 DVS1_POL: DVS1 pin polarity
0: active low
1: active high

Bit 0 INT_POL: INT pin polarity
0: active low
1: active high

15.2.5.6 DCDC_ILMAX_REG : DCDC max inductor current Register

Address: 90H				Type: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BUCK4_ILMAX		BUCK3_ILMAX		BUCK2_ILMAX		BUCK1_ILMAX	
Default	0	1	0	1	0	1	0	1

Description

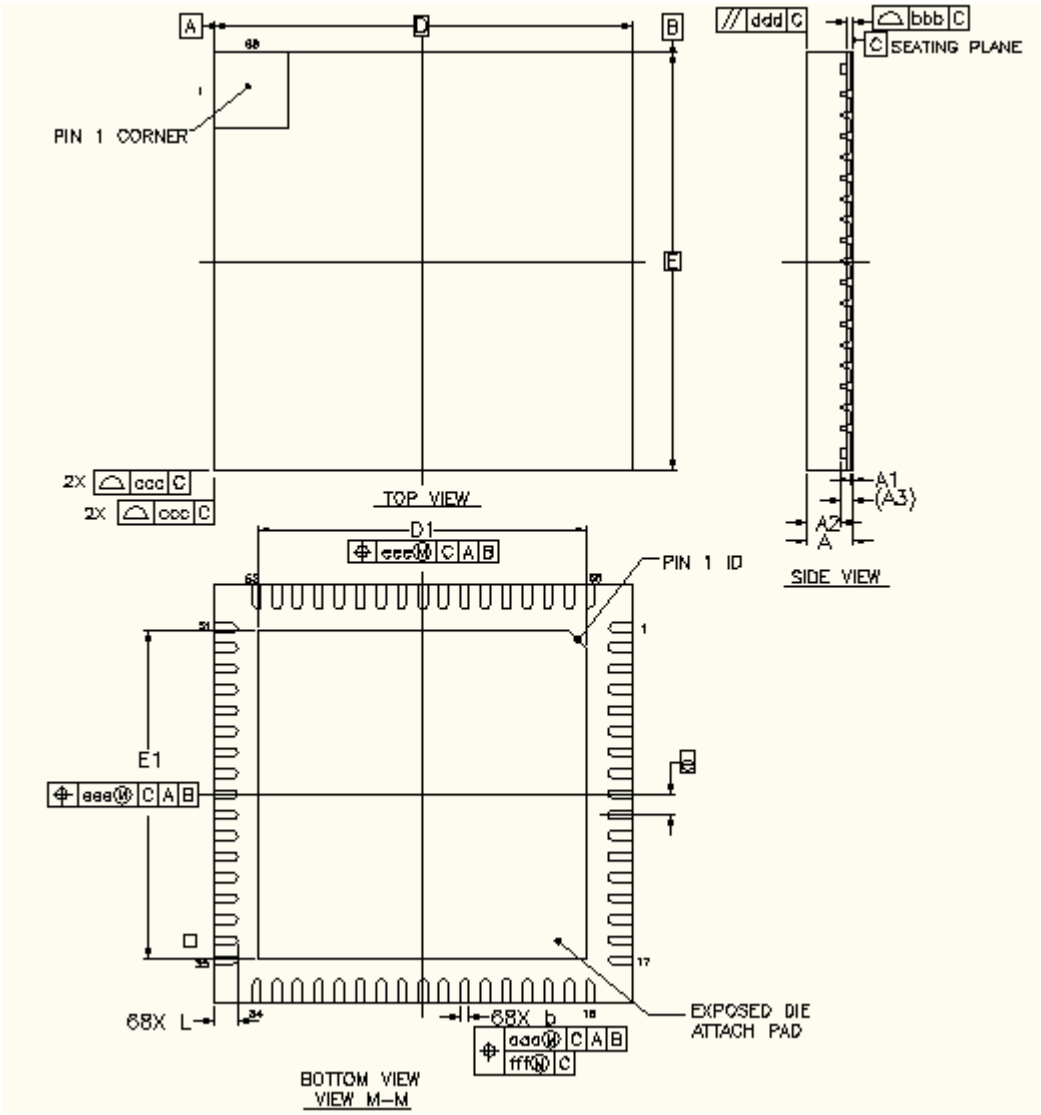
Bit 7-6 BUCK4_ILMAX: BUCK4 max inductor current
00:2A 01:2.5A 10:3A 11:3.5A

Bit 5-4 BUCK3_ILMAX: BUCK4 max inductor current
00:2A 01:2.5A 10:3A 11:3.5A

Bit 3-2 BUCK2_ILMAX: BUCK4 max inductor current
00:4.5A 01: 5A 10:5.5A 11:6A

Bit 1-0 BUCK1_ILMAX: BUCK4 max inductor current
00:4.5A 01: 5A 10:5.5A 11:6A

16 PACKAGE INFORMATION



QFN68 7mm X 7mm

DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.035	0.05

MOLD THICKNESS	A2	-	0.55	0.57
MATERIAL THICKNESS	A3	-	0.203_{REF}	-
PACKAGE SIZE	D	-	7_{BSC}	-
	E	-	7_{BSC}	-
EP SIZE	D1	5.39	5.49	5.59
	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.4	0.50
LEAD PITCH	e	0.35_{BSC}		
LEAD WIDTH	b	0.1	0.15	0.2
LEAD OSITION OFFSET	aaa	0.07		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.10		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		

Note:

1. Coplanarity applies to leads, corner leads and die attach pad.
2. Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.
3. 0.15mm of dimension b is recommended in PCB layout.