Reference Schematic For PX30 MINI

PX30_MINI_EVB_V1.0

PMIC: RK809-1 (5BUCK + 9LDO + Codec)
RAM: DDR3 /LPDDR3/DDR4
ROM: eMMC/Nand + TF card
Interface: MIPI CSI/MIPI DSI/UART/I2S/RMII

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	00.Cover Page		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	1 of 32

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Note

NOTE 1:
Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:
Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

Note

Option

Description

Remind

Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	01.Index		
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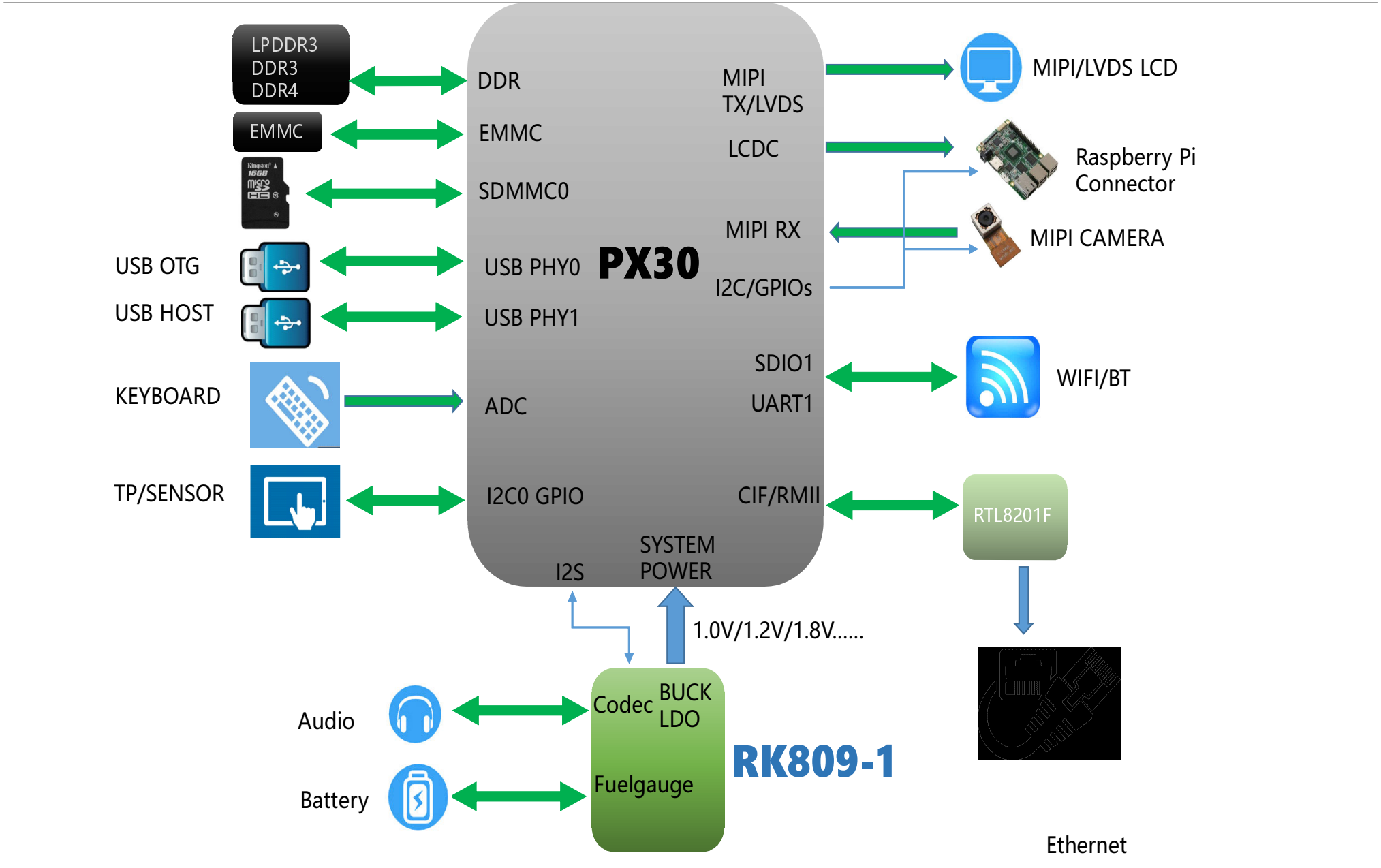
Version	Date	Author	Change List	Approved
V1.0	20180504	XHF	First edition for PX30	

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics			
Project:	PX30 MINI EVB		
File:	02.Revision History		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	3 of 32



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	03.Block Diagram		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	4 of 32

I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL/GPIO0_B0_u I2C0_SDA/GPIO0_B1_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC3V0_PMU	Rockchip RK809	0x20	PMIC	
I2C1	I2C1_SCL/PMU_DEBUG5/GPIO0_C2_u I2C1_SDA/GPIO0_C3_u	PMUIO2	I2C1_SCL I2C1_SDA	VCC3V0_PMU	MMA8452Q	0x1d	Accelerometer	100kHz,400kHz
					LIS3DH	0x19	Accelerometer	100kHz,400kHz
					LSM303D	0x1d	Accelerometer+Magnetic	100kHz,400kHz
I2C2	I2C2_SCL/GPIO2_B7_u I2C2_SDA/GPIO2_C0_u	VCCIO3	I2C2_SCL_CAM I2C2_SDA_CAM	VCC_RMII	OV5695	0X36	MIPI Camera	

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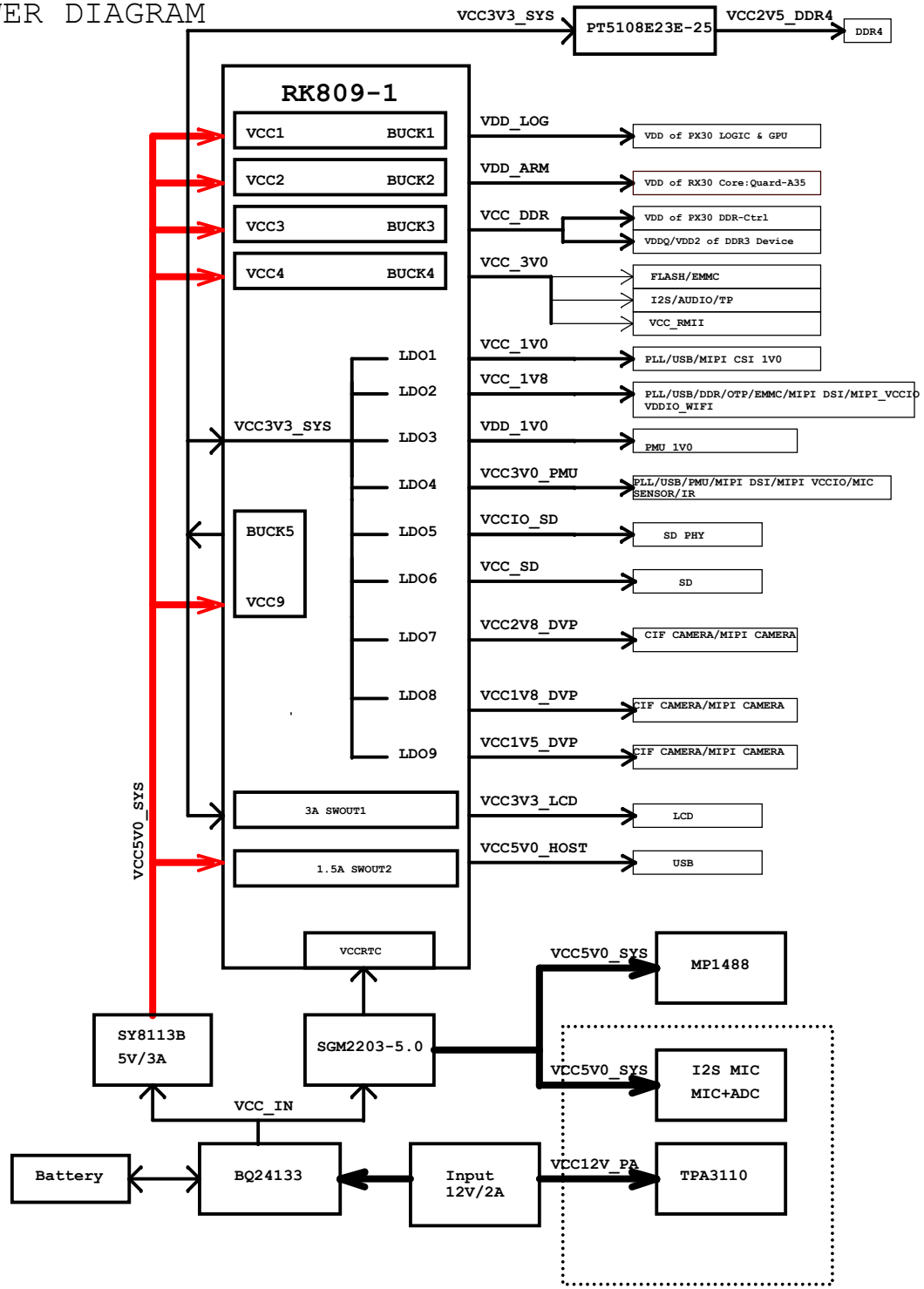
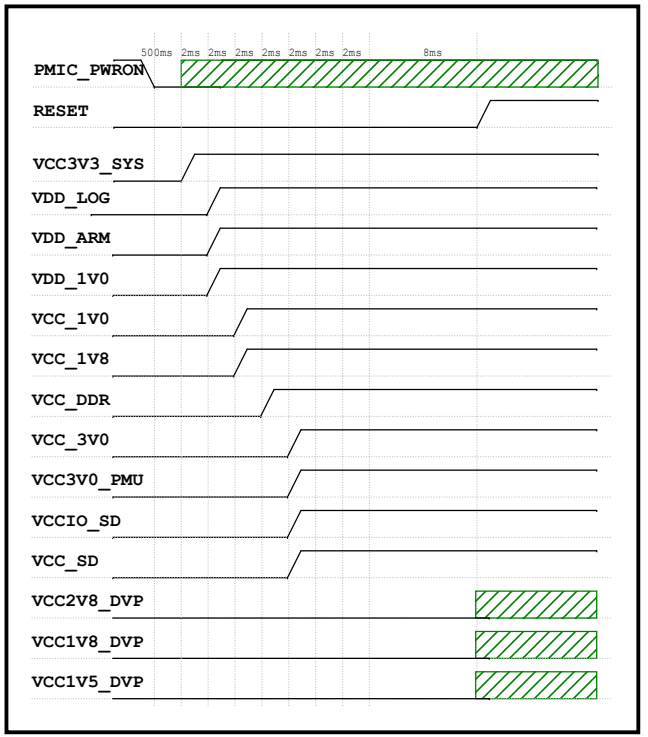
Project:	PX30 MINI EVB		
File:	04.I2C MAP		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	5 of 32

POWER DIAGRAM

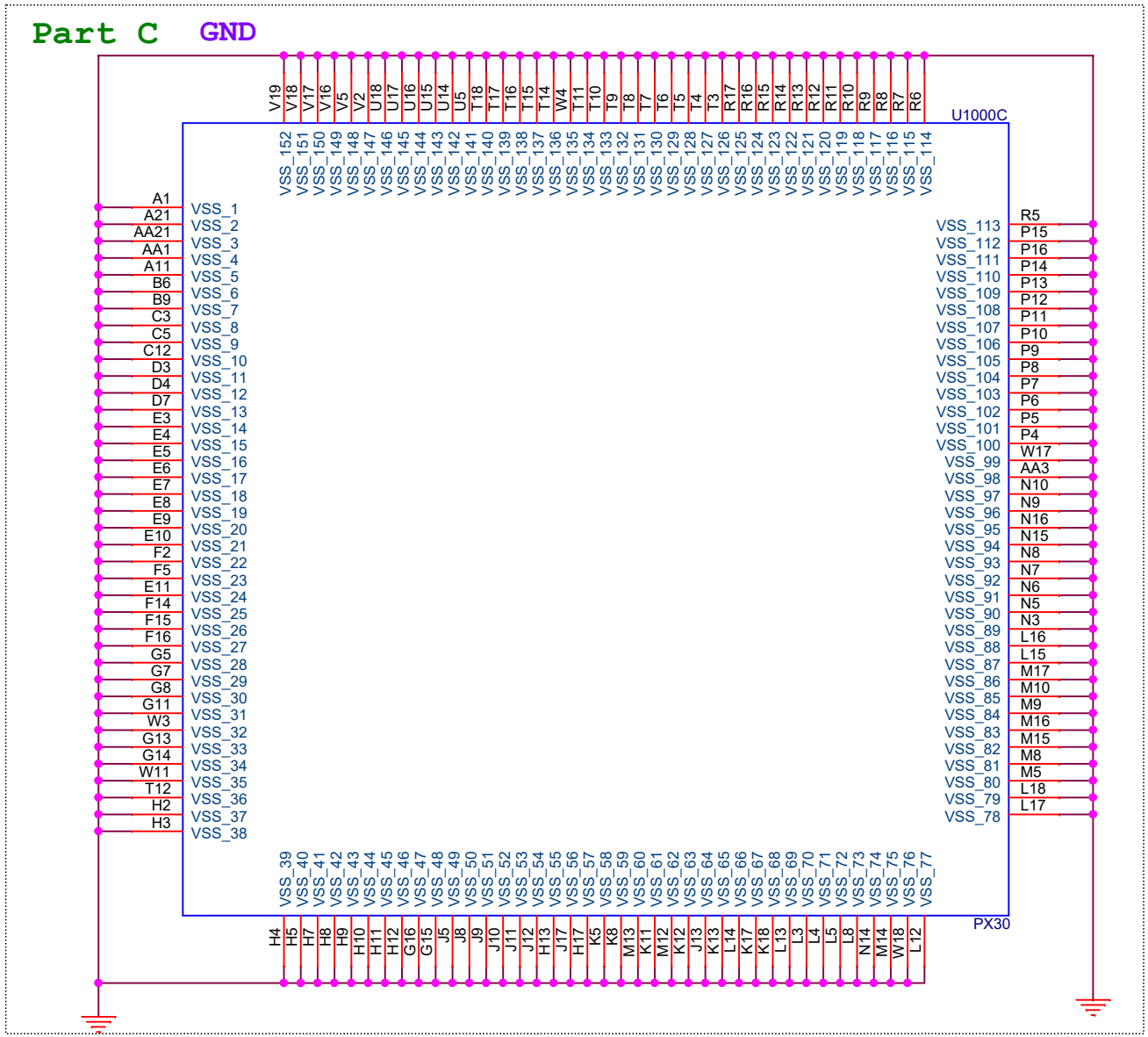


RK809-1 Power-on Sequence

PowerName	PMIC Channel	Time Slot (step 2mS)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VDD_ARM	BUCK1	Slot:2	1.0V	2.5A	ON	OFF	1160mA
VDD_LOG	BUCK2	Slot:2	1.0V	2.5A	ON		1020mA
VCC_DDR	BUCK3	Slot:4	FB=0.6V	1.5A	ON	ON	790mA
VCC_3V0	BUCK4	Slot:5	3.0V	1.5A	ON	ON	360mA
VCC3V3_SYS	BUCK5	Slot:1	3.3V	1.5A	ON	ON	
VCC_1V0	LDO1	Slot:3	2.5V	500mA	ON	ON	
VCC_1V8	LDO2	Slot:3	1.8V	500mA	ON	ON	236mA
VDD_1V0	LDO3	Slot:2	1.0V	500mA	ON	ON	13.6mA
VCC3V0_PMU	LDO4	Slot:5	3.0V	100mA	ON	ON	9mA
VCCIO_SD	LDO5	Slot:5	3.0V	500mA	ON		
VCC_SD	LDO6	Slot:5	3.0V	500mA	ON		
VCC2V8_DVP	LDO7		2.8V	500mA	OFF	OFF	
VCC1V8_DVP	LDO8		1.8V	500mA	OFF	OFF	
VCC1V5_DVP	LDO9		1.5V	500mA	OFF	OFF	
RESET	RESETB	Slot:11	OD				

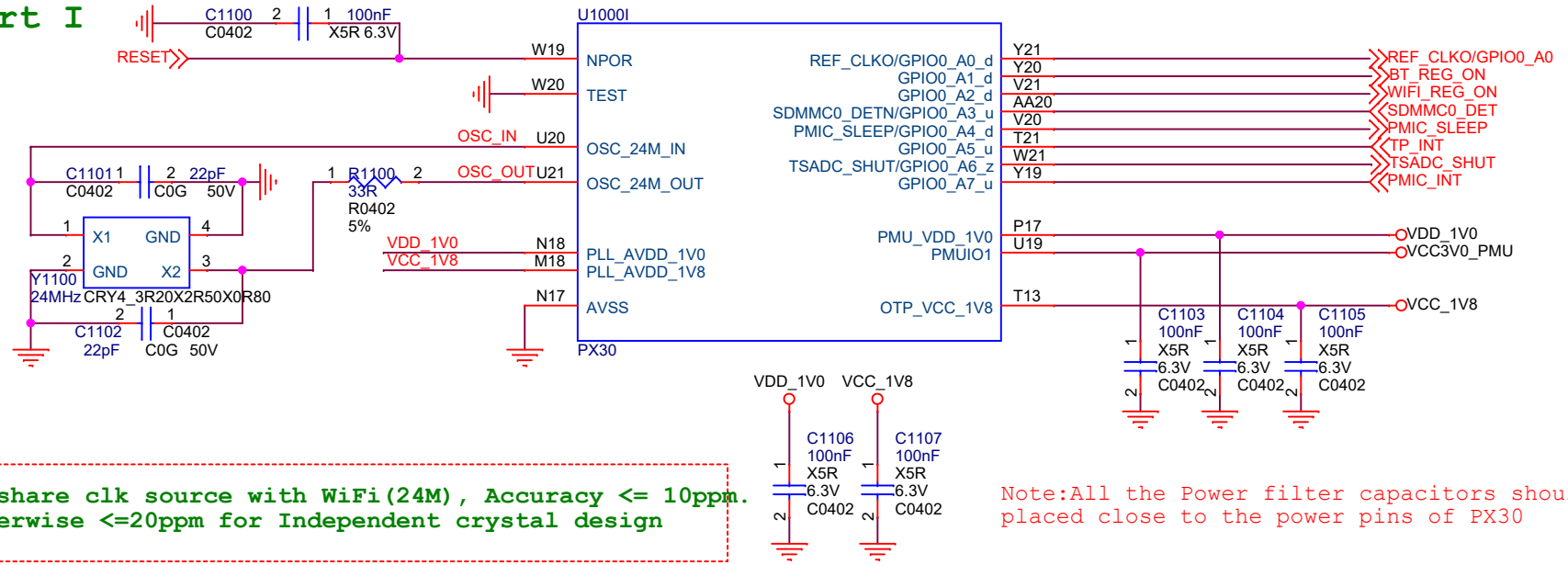


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	05.Power diagram and Sequence		
Date:	Thursday, September 27, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	6 of 32



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	10.PX30 Power		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	7 of 32

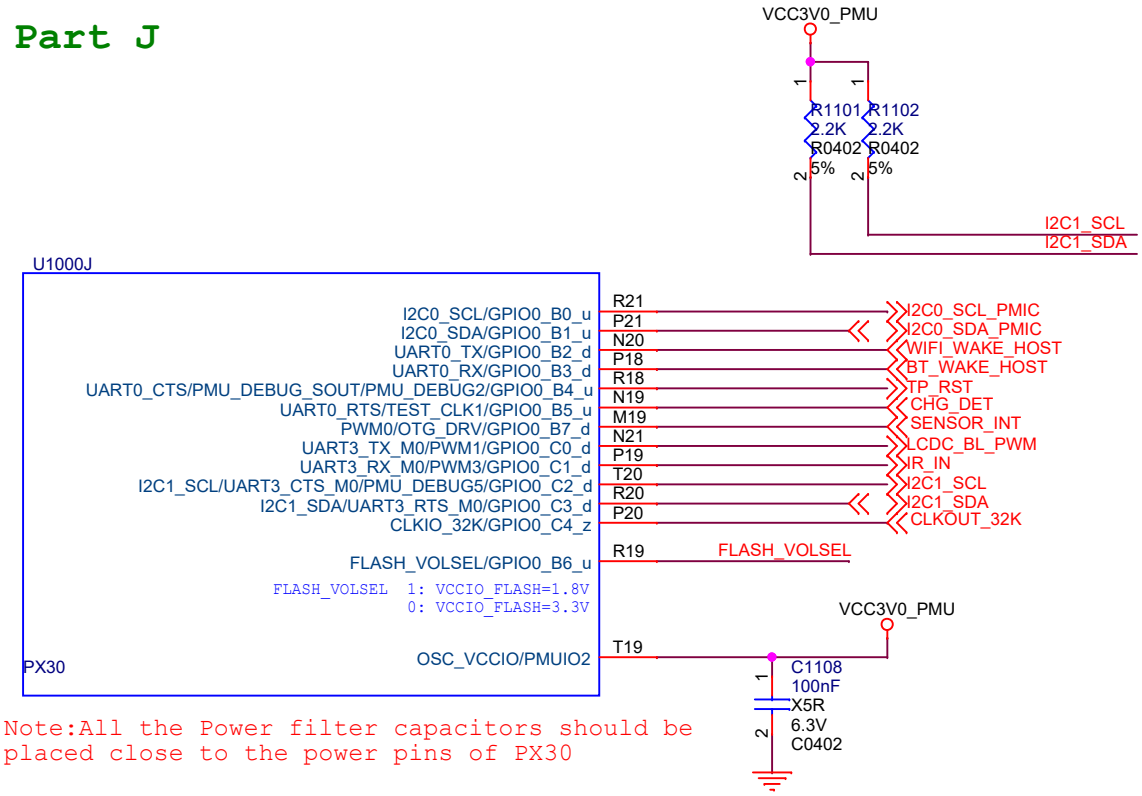
Part I



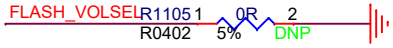
If share clk source with WiFi(24M), Accuracy <= 10ppm.
Otherwise <=20ppm for Independent crystal design

Note:All the Power filter capacitors should be placed close to the power pins of PX30

Part J



Note:All the Power filter capacitors should be placed close to the power pins of PX30



Floating or Pull-up FLASH_VOLSEL=1	Pull-down FLASH_VOLSEL=0
VCCIO_FLASH=1.8V	VCCIO_FLASH=3.3V

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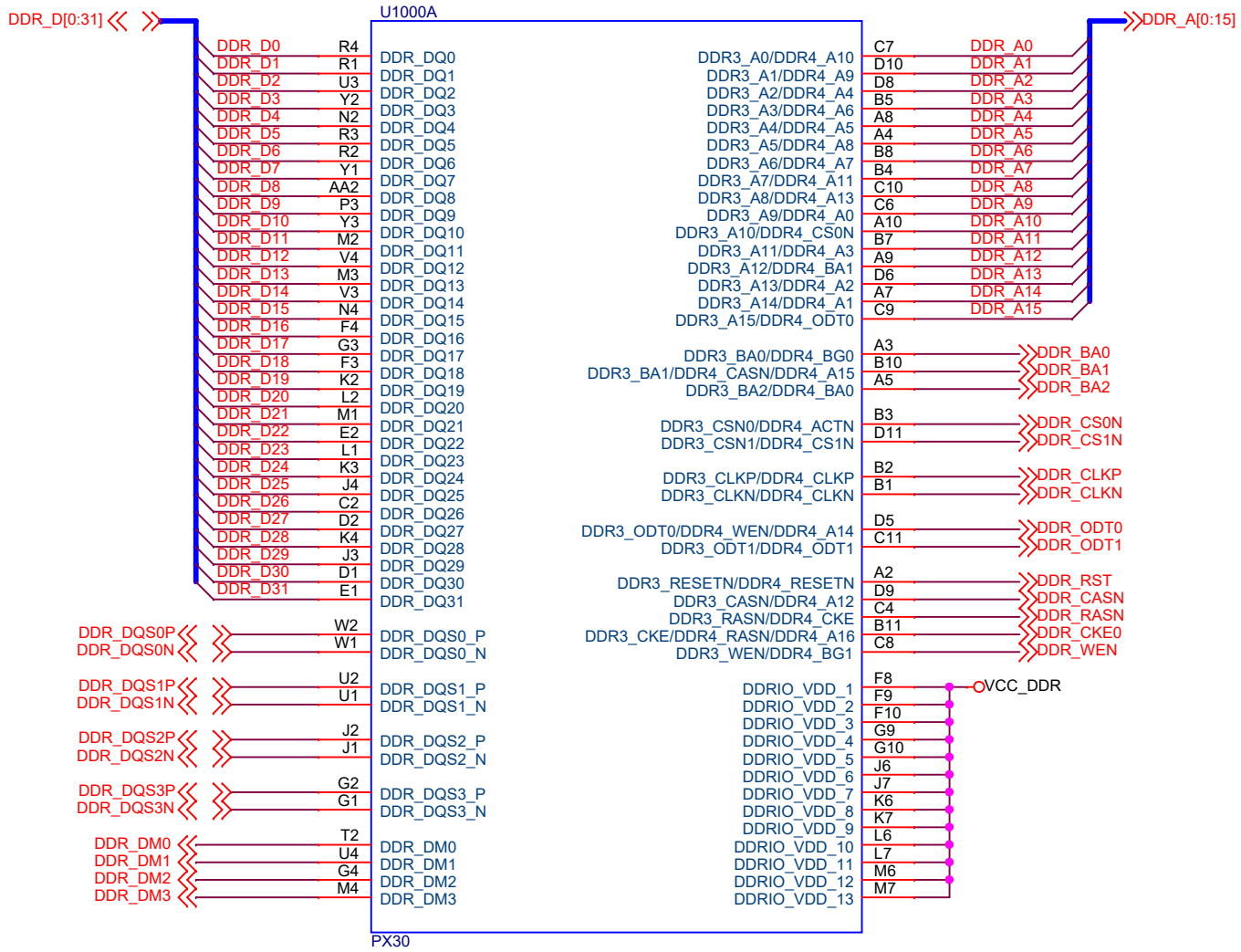
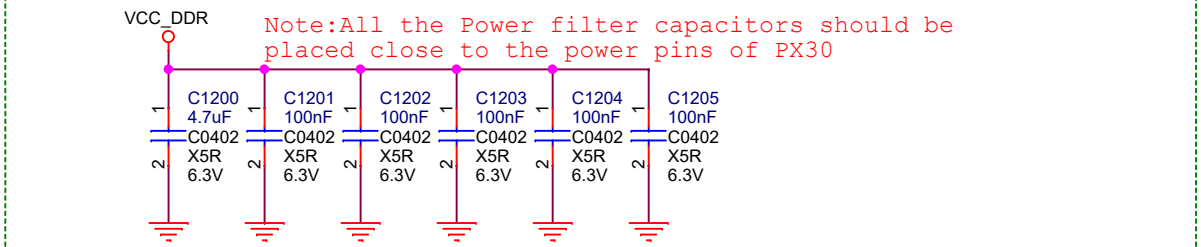
Project:	PX30 MINI EVB		
File:	11.PX30 OSC/PMUIO		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	8 of 32

Part A DDR Controler



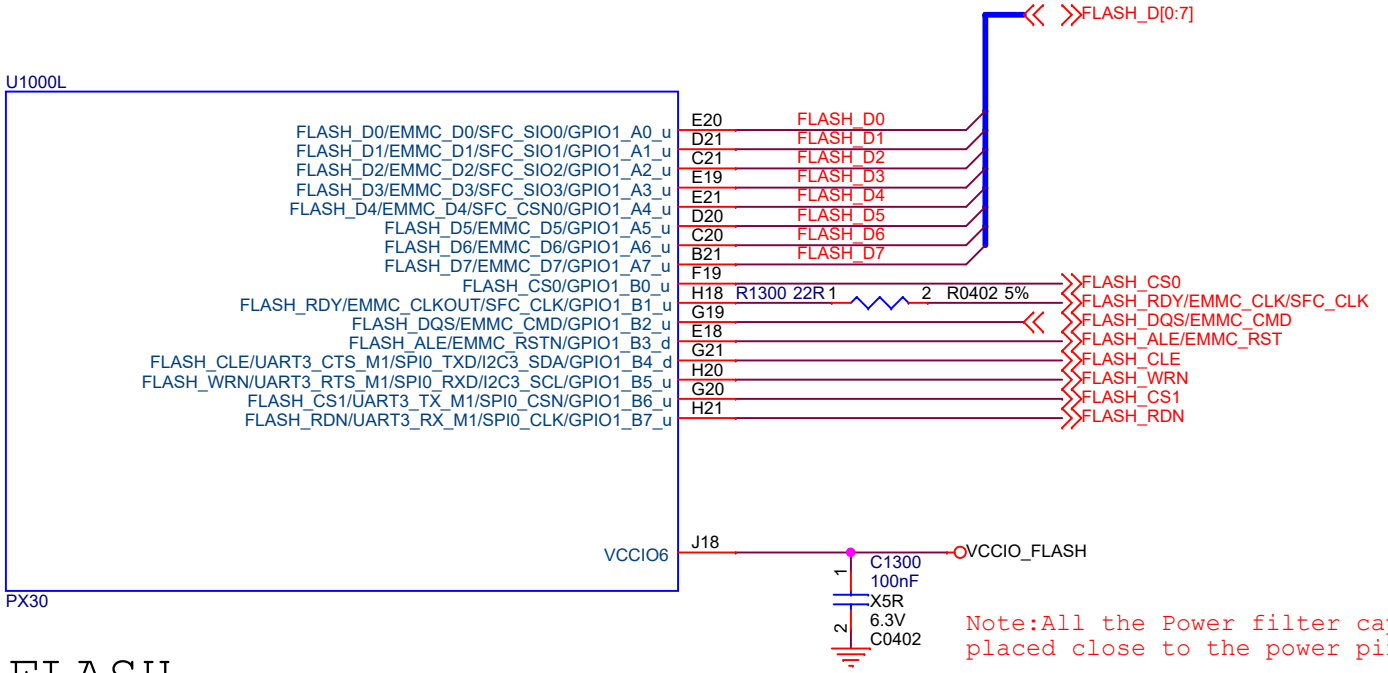
DDR3/DDR4 PIN MUX

DDR3_A0	DDR4_A10
DDR3_A1	DDR4_A9
DDR3_A2	DDR4_A4
DDR3_A3	DDR4_A6
DDR3_A4	DDR4_A5
DDR3_A5	DDR4_A8
DDR3_A6	DDR4_A7
DDR3_A7	DDR4_A11
DDR3_A8	DDR4_A13
DDR3_A9	DDR4_A0
DDR3_A10	DDR4_CS0n
DDR3_A11	DDR4_A3
DDR3_A12	DDR4_BA1
DDR3_A13	DDR4_A2
DDR3_A14	DDR4_A1
DDR3_A15	DDR4_ODT0
DDR3_BA0	DDR4_BG0
DDR3_BA1	DDR4_CASn/DDR4_A15
DDR3_BA2	DDR4_BA0
DDR3_CS0N	DDR4_ACTn
DDR3_CS1N	DDR4_CS1N
DDR3_ODT0	DDR4_WEn/DDR4_A14
DDR3_ODT1	DDR4_ODT1
DDR3_CLKP	DDR4_CLKP
DDR3_CLKn	DDR4_CLKn
DDR3_CKE	DDR4_RASn/DDR4_A16
DDR3_RASn	DDR4_CKE
DDR3_CASN	DDR4_A12
DDR3_WEn	DDR4_BG1
DDR3_RST	DDR4_RST



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	12.PX30 DDR Controller		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	9 of 32

Part L

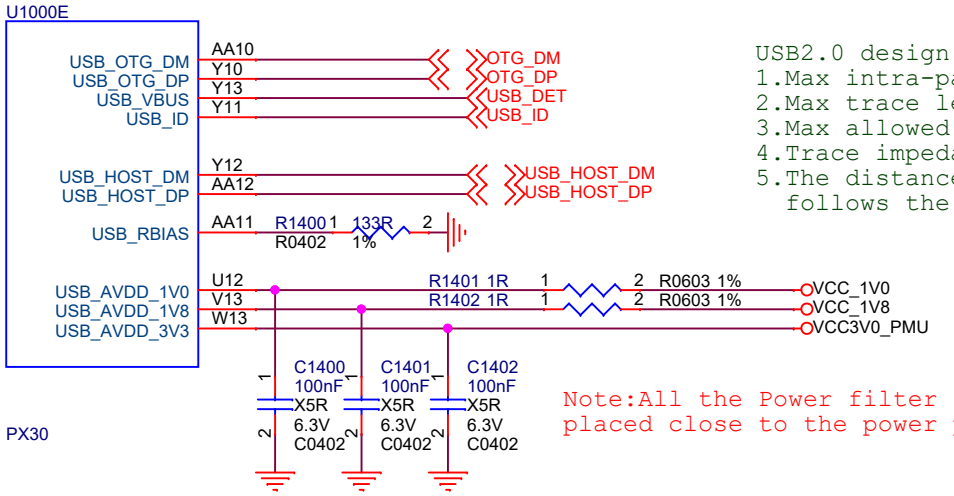


FLASH

Note:All the Power filter capacitors should be placed close to the power pins of PX30

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	13.PX30 Flash Controller		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	10 of 32

Part E



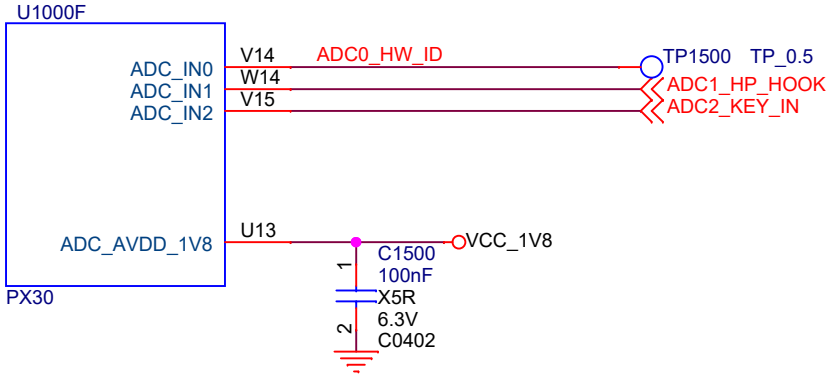
USB2.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

Note:All the Power filter capacitors should be placed close to the power pins of PX30

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	14.PX30 USB Controller		
Date:	Thursday, August 30, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	11 of 32

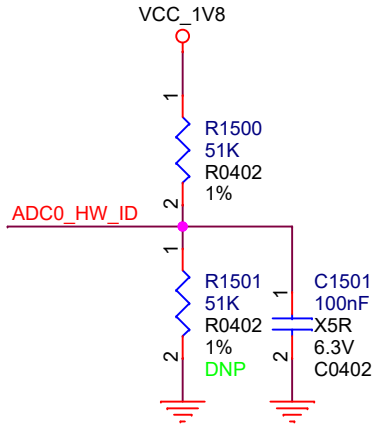
ADC0_HW_ID

Part F



Note:All the Power filter capacitors should be placed close to the power pins of PX30

It is reserved for the hardware version of the product.
If it is not needed, it can be removed.

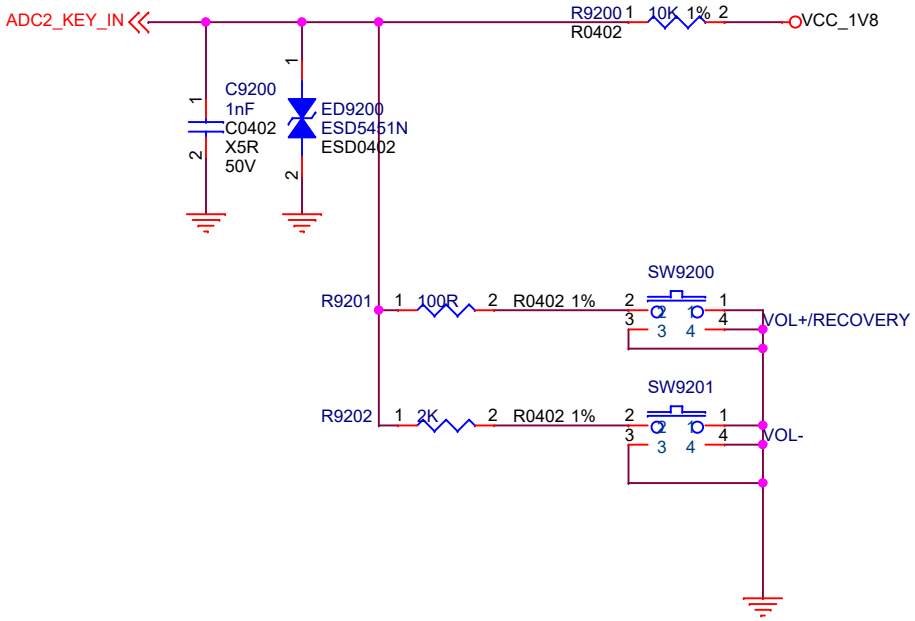


HW ID

ADC0_HW_ID	Pull-up Resistance	Pull-down Resistance	ADC Value
Version0 (Default)	51K	DNP	1024

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	**PX30 MINI EVB**		
File:	**15.PX30 ADC**		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	12 of 32

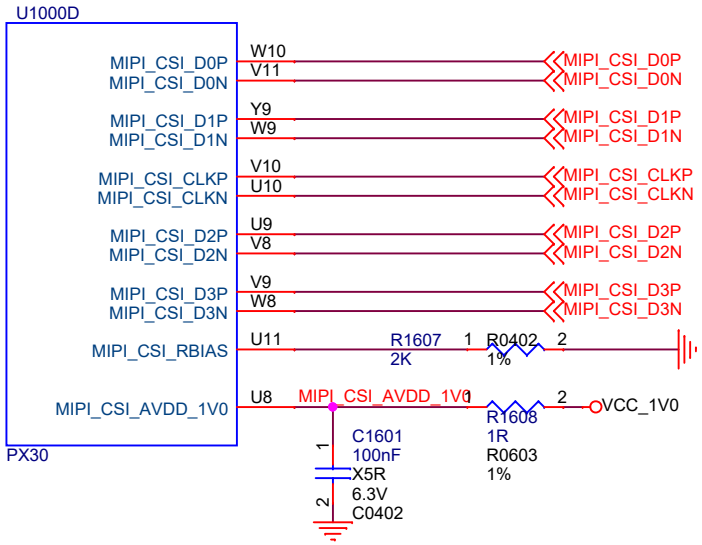
KEY BAORD



Key Name	SARADC
VOL+/RECOVERY	10
VOL-	170

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	92.KEY Board		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	12 of 14

Part D

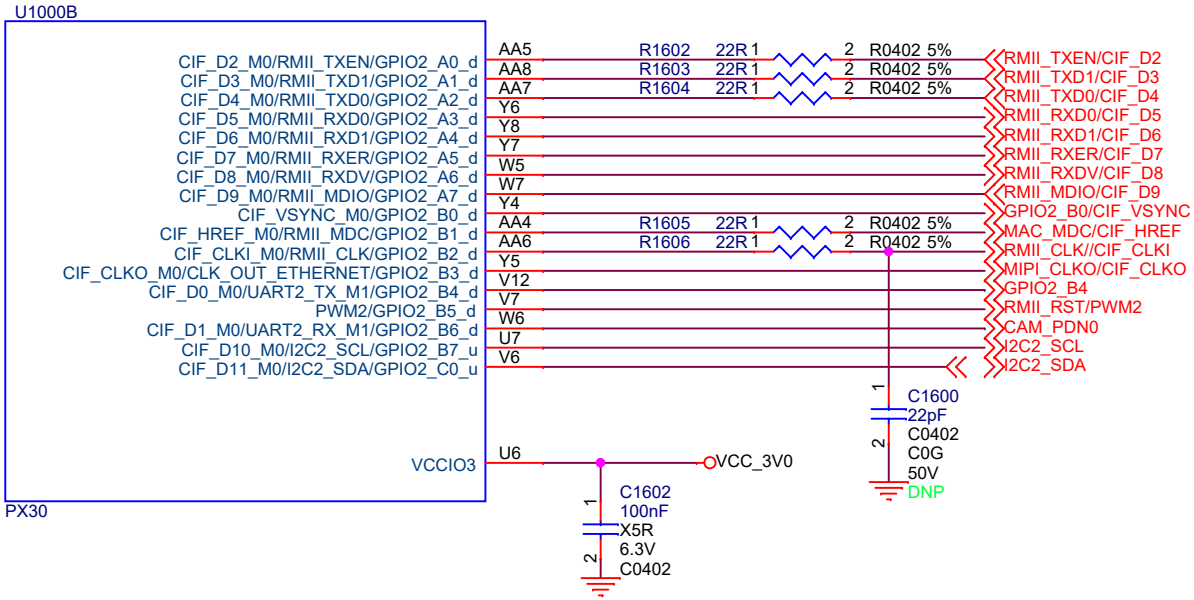


Note:All the Power filter capacitors should be placed close to the power pins of PX30

MIPI CSI

MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

Part B



CIF/RMII

Note:All the Power filter capacitors should be placed close to the power pins of PX30

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	16.PX30 DVP Interface		
Date:	Monday, May 28, 2018	Rev:	V1.0
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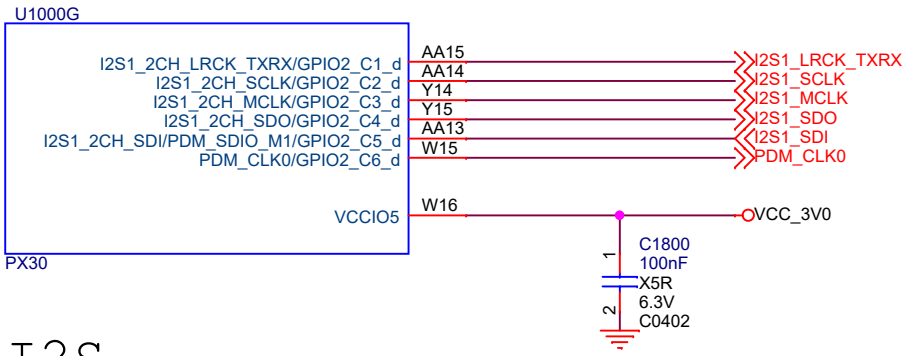
Part M

MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

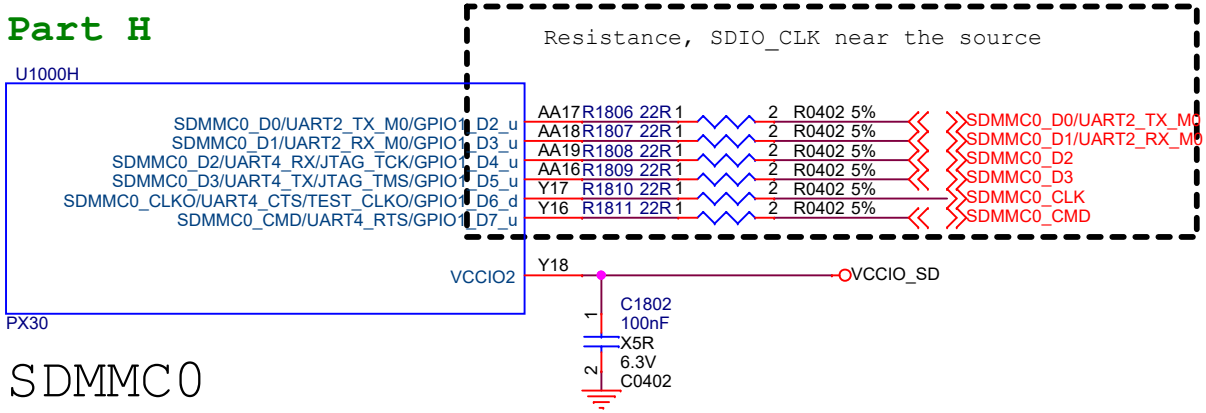
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	17.PX30 MIPI DSI/LCDC		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	14 of 32

Part G



I2S

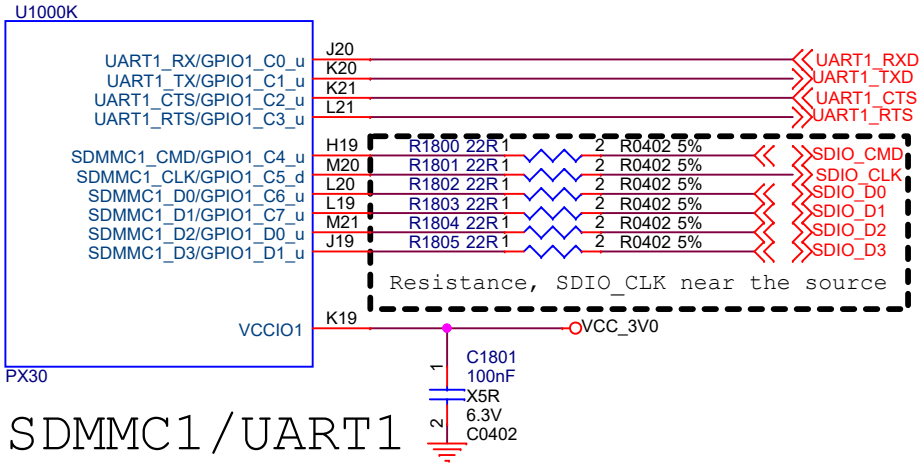
Part H



SDMMC0

Note:All the Power filter capacitors should be placed close to the power pins of PX30

Part K

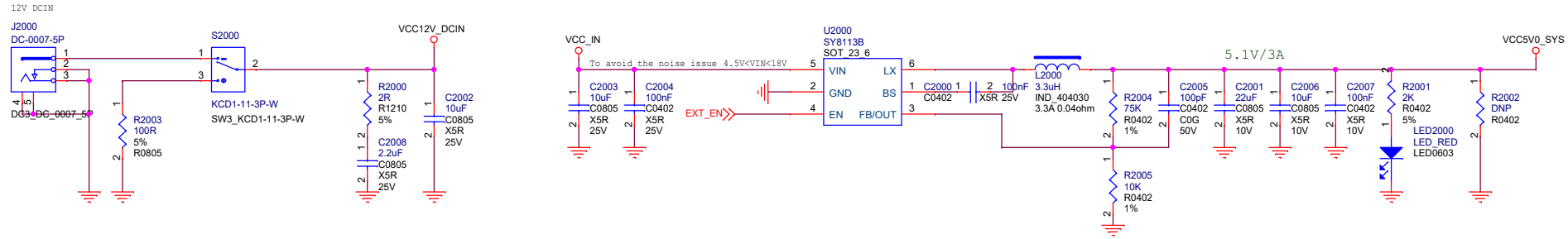


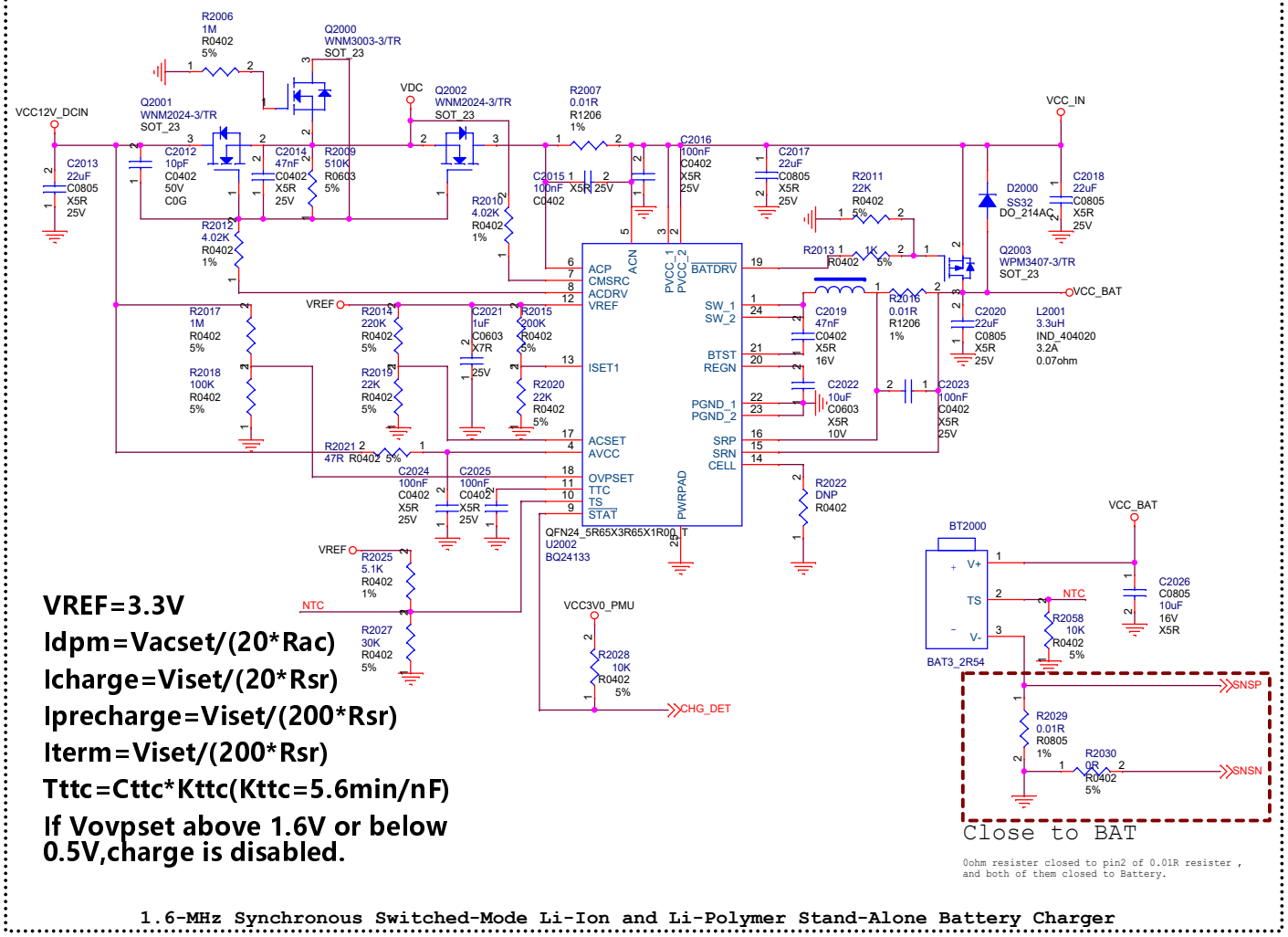
SDMMC1/UART1

Note:All the Power filter capacitors should be placed close to the power pins of PX30

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	18.PX30 I2S/SDMMC0/SDMMC1		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	15 of 32

DC IN&SYSTEM Power





VREF=3.3V

Idpm=Vacset/(20*Rac)

Icharge=Viset/(20*Rsr)

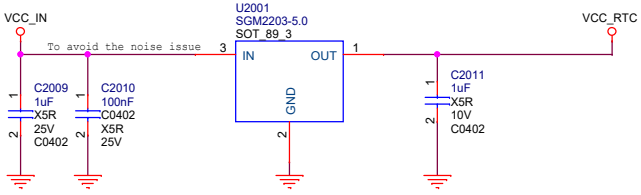
Iprecharge=Viset/(200*Rsr)

Iterm=Viset/(200*Rsr)

Tttc=Cttc*Kttc(Kttc=5.6min/nF)

If Vovpset above 1.6V or below 0.5V,charge is disabled.

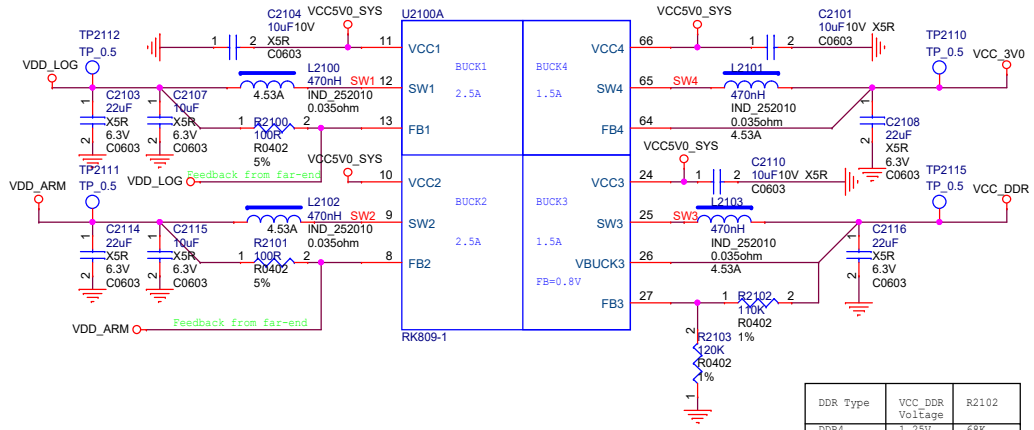
1.6-MHz Synchronous Switched-Mode Li-Ion and Li-Polymer Stand-Alone Battery Charger



LDO-VCCRTC

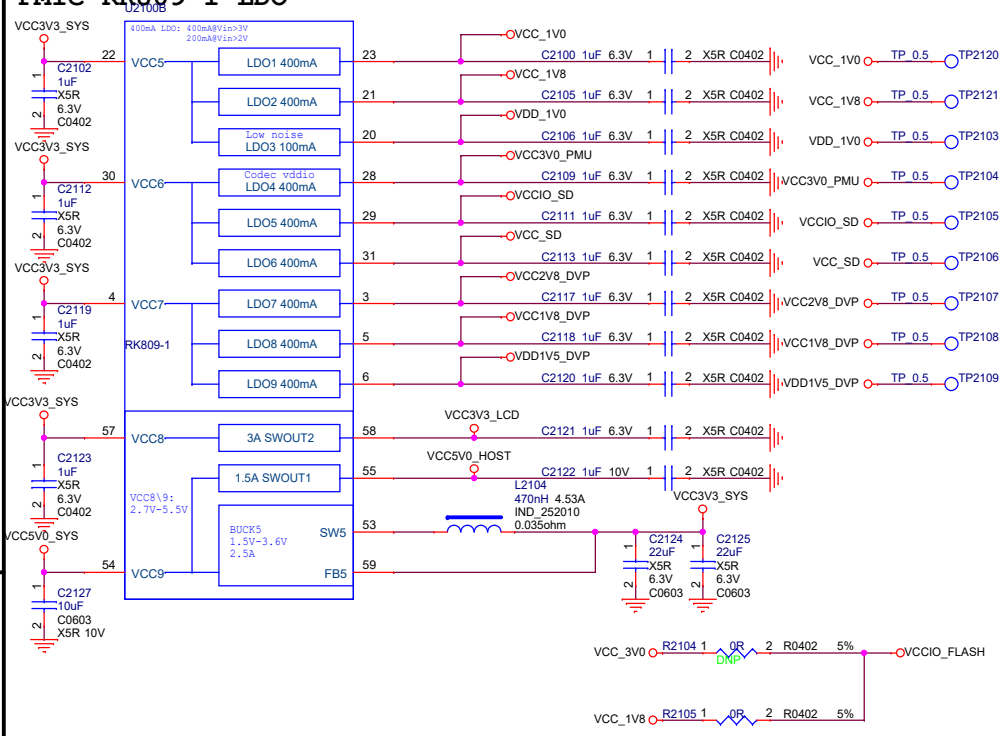
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	20.Power-DC IN		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	16 of 32

PMIC RK809-1 DCDC

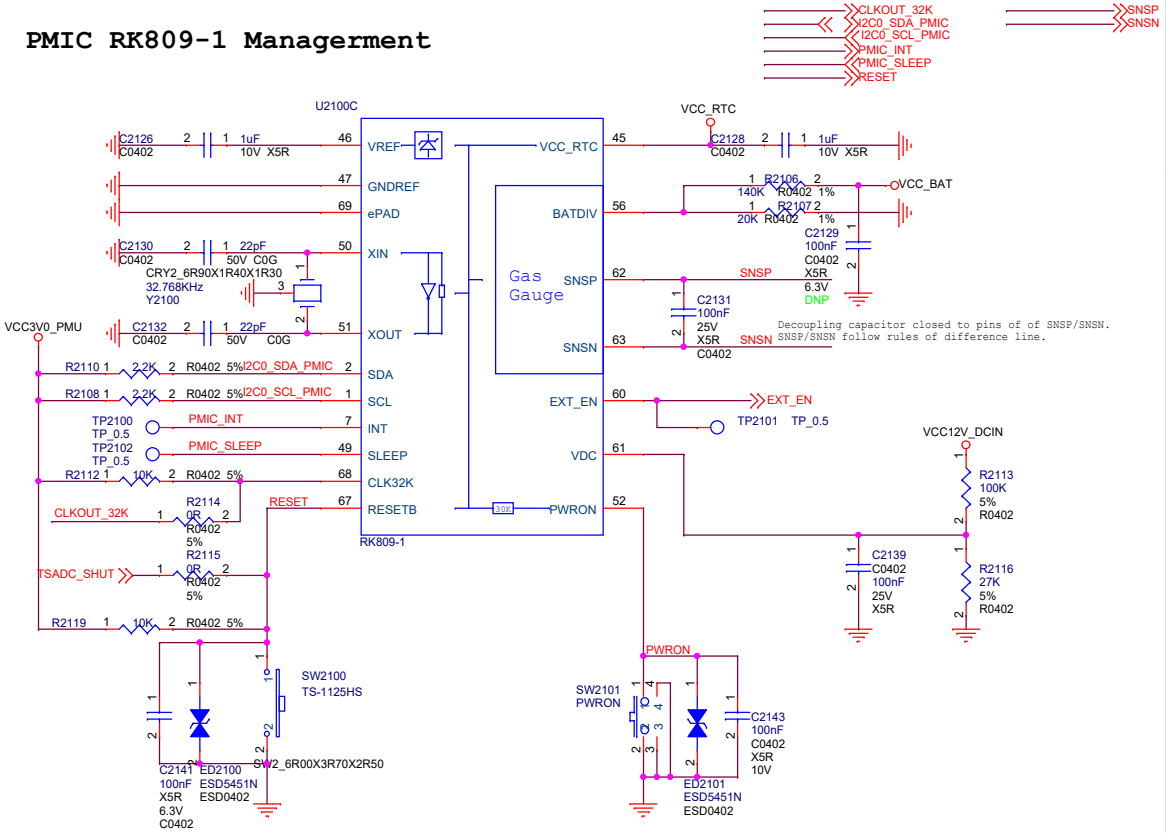


DDR Type	VCC_DDR Voltage	R2102
DDR4	1.25V	68K
LPDDR3	1.25V	68K
DDR3L	1.35V	82K
DDR3	1.53V	110K

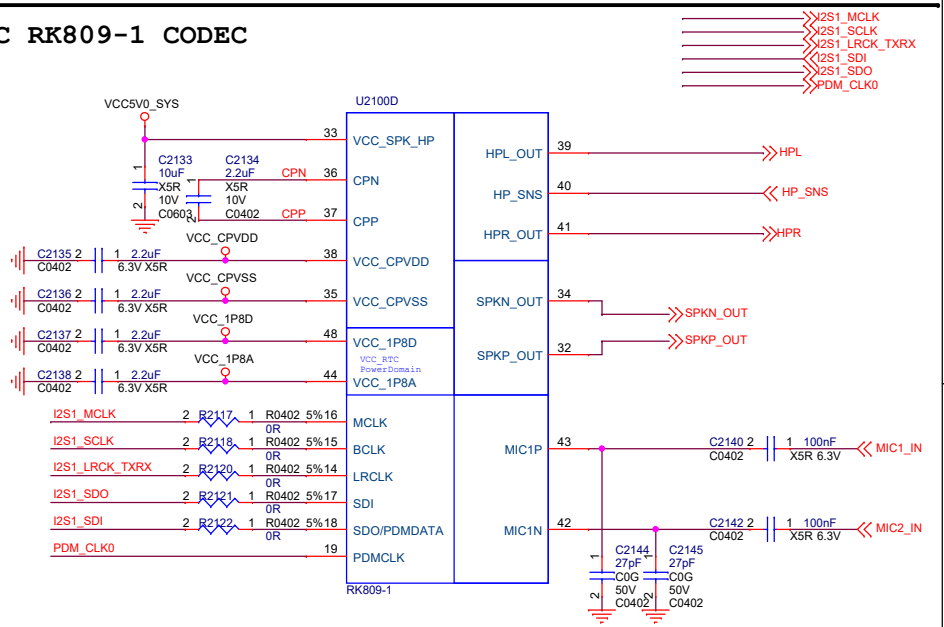
PMIC RK809-1 LDO



PMIC RK809-1 Managerment

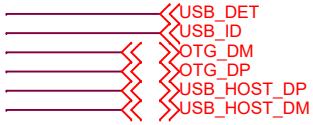


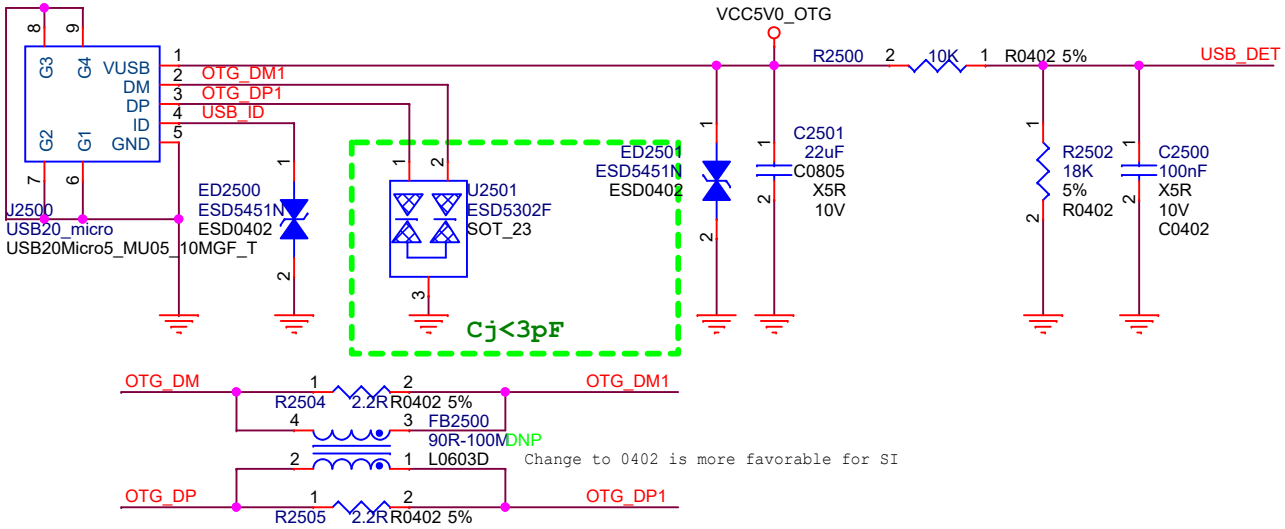
PMIC RK809-1 CODEC

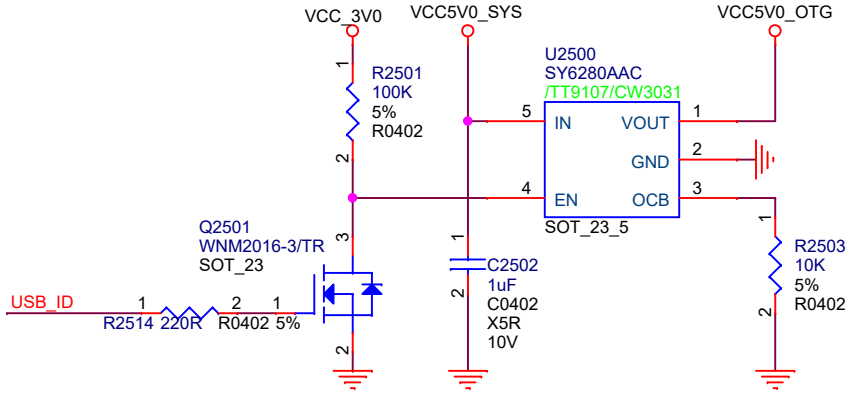


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	21:Power-PMIC RK809-1		
Date:	Thursday, September 27, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	17 of 32

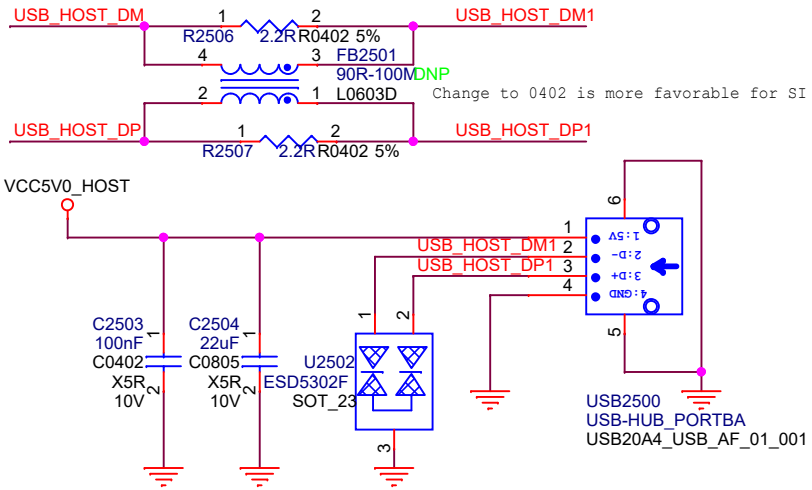
USB OTG







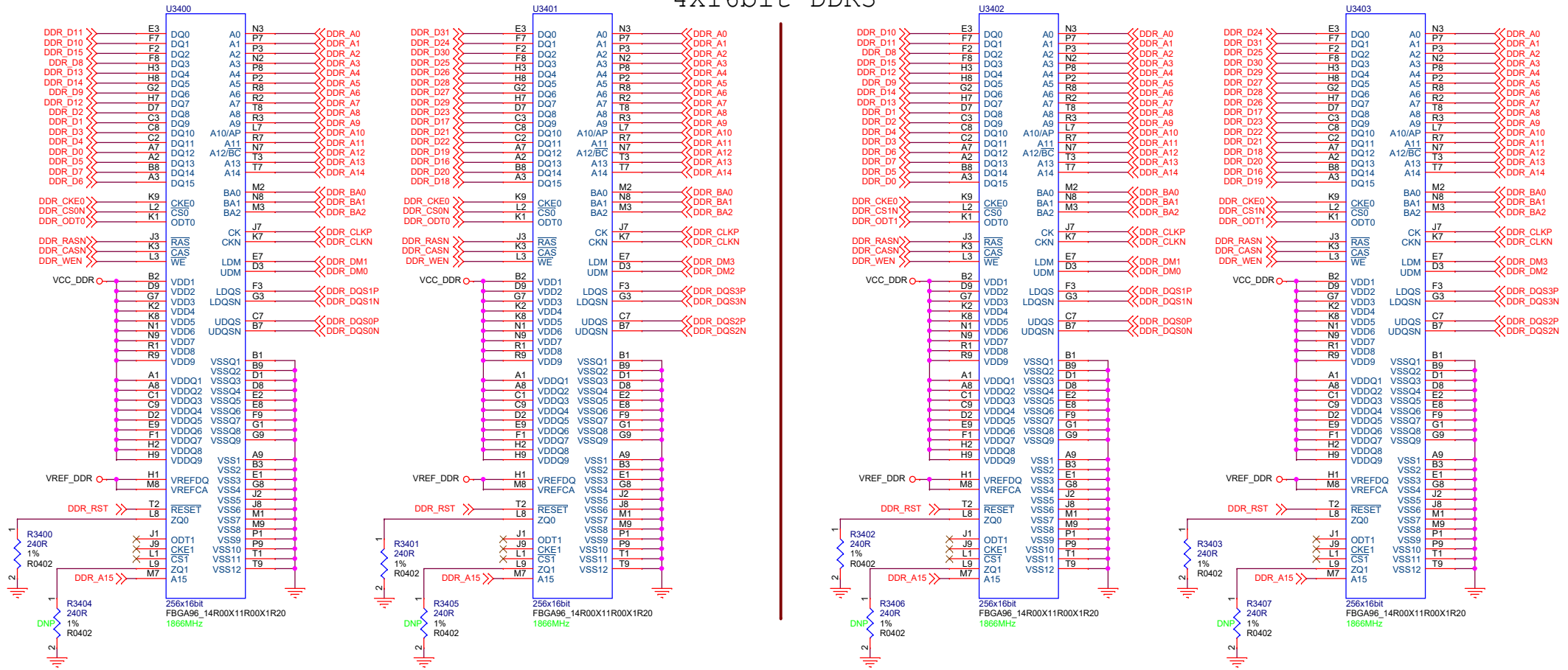
USB HOST



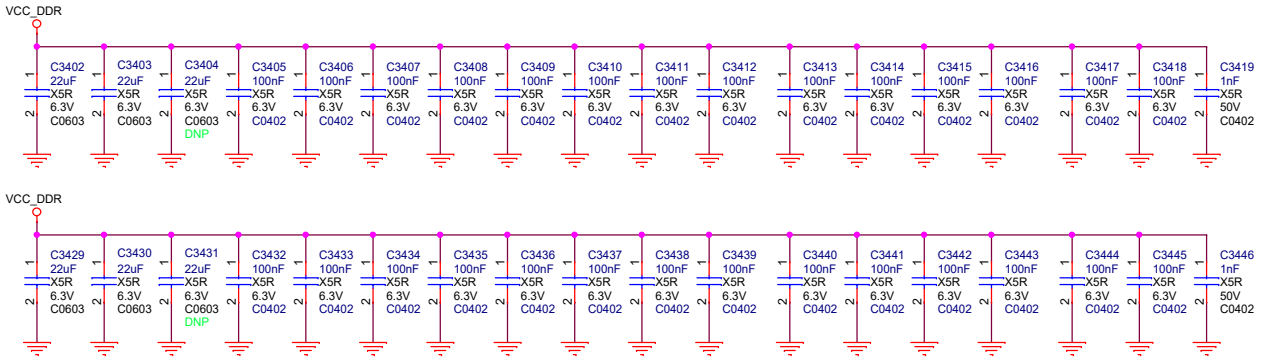
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	25.USB OTG/HOST		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	18 of 32

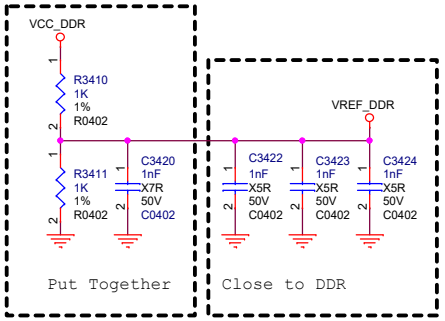
Note:The simulation frequency of the template is 533MHz.

4X16bit DDR3



DDR3 FILTER





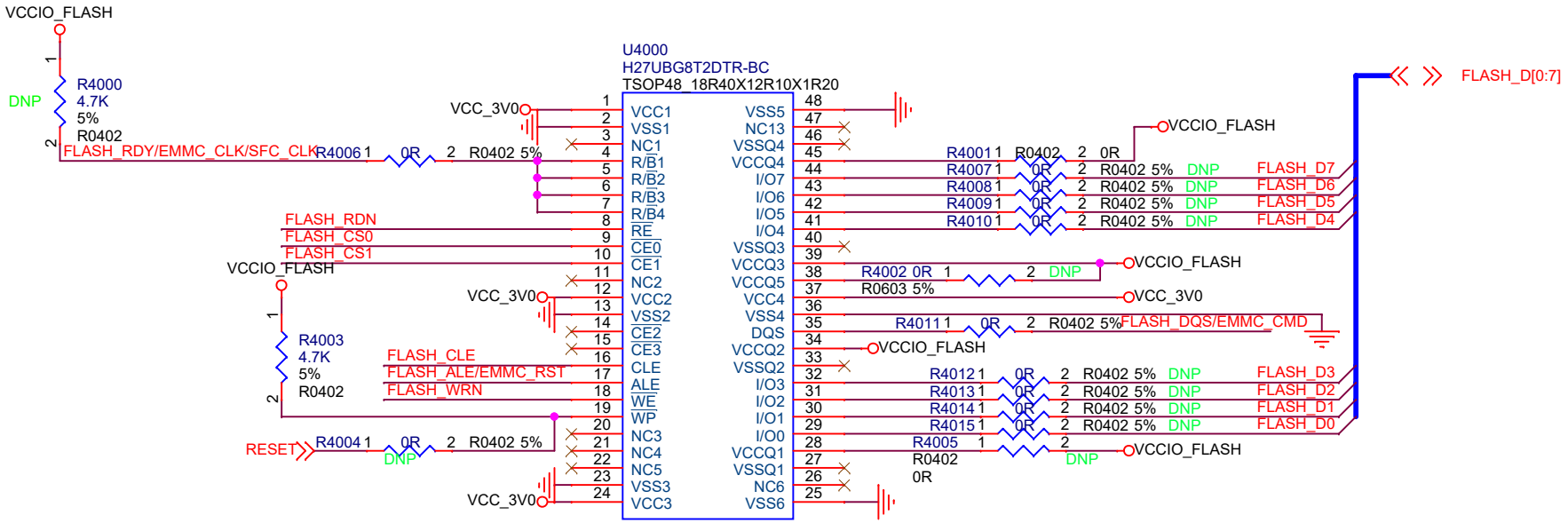
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	RAM DDR3 4x16bit		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	19 of 32

Nand Flash

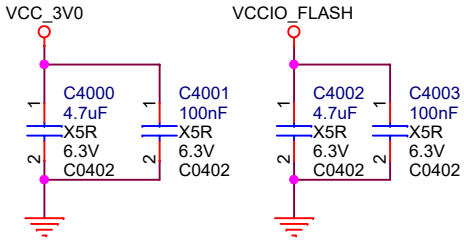
Remind: Refer to the latest AVL for parts selection.

FLASH_RDN
FLASH_RDY/EMMC_CLK/SFC_CLK
FLASH_WRN
FLASH_CLE
FLASH_ALE/EMMC_RST
FLASH_DQS/EMMC_CMD
FLASH_CS0
FLASH_CS1

Note:Flash_RDY pull-up resister must
be deleted in eMMC Flash mode and
be mounted in Nand Flash mode.

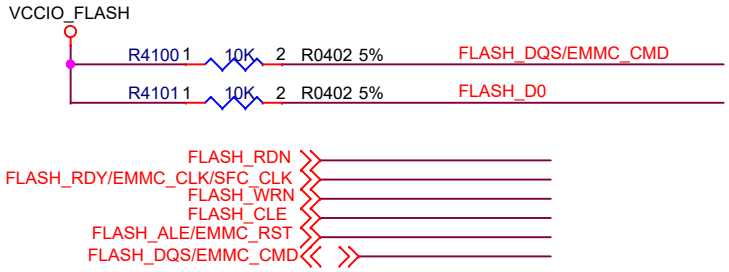


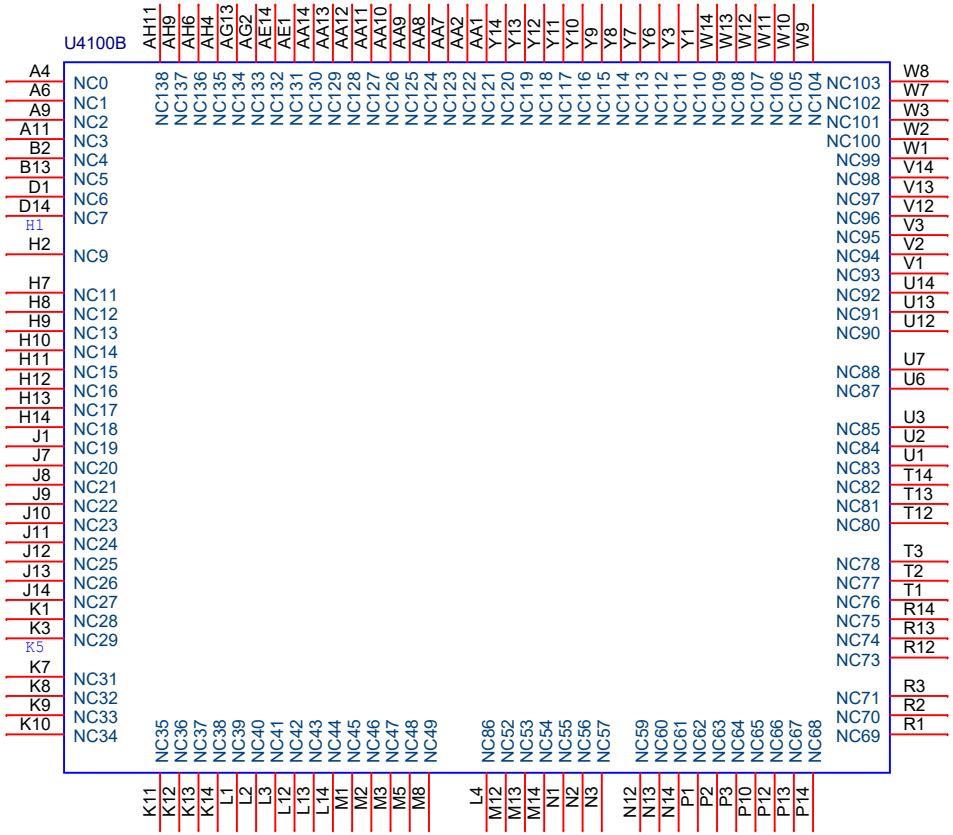
Note: if use toshiba and sandisk DDR mode,
VCCQ1 and VCCQ4 must be connected to VCC_IO。



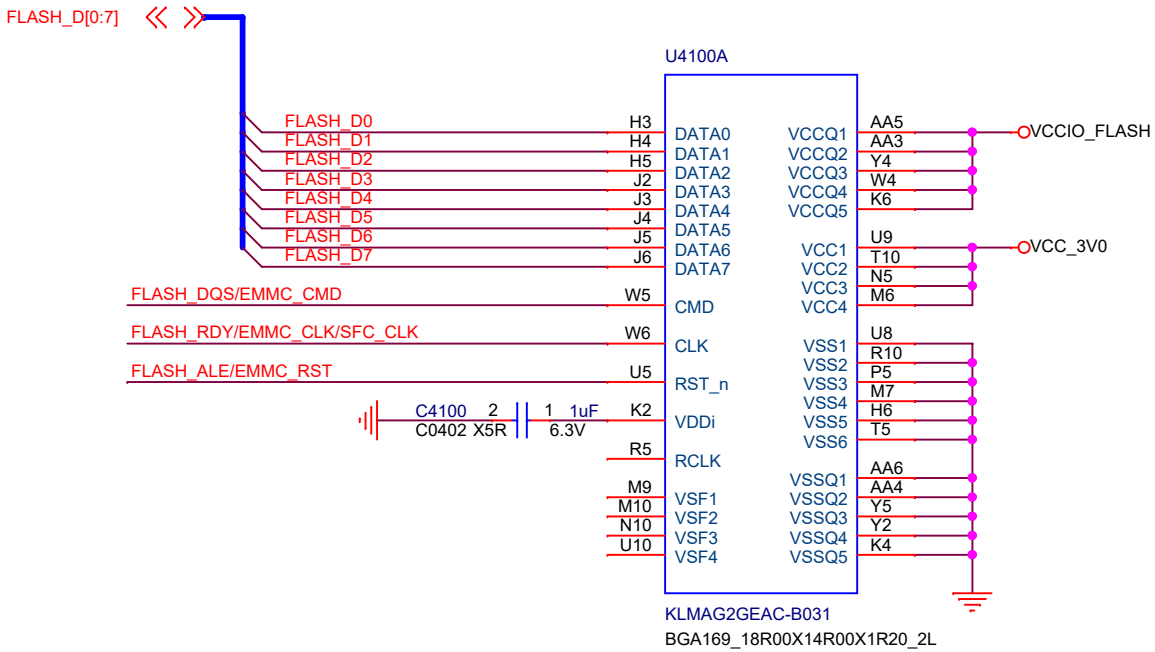
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	40.Flash-Nand Flash(option)		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	20 of 32

eMMC

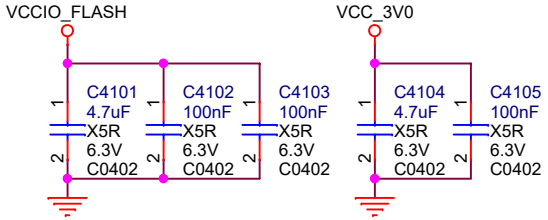


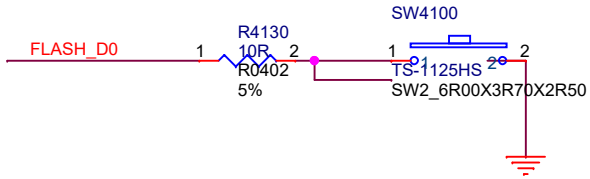


BGA169_18R00X14R00X1R20_2L
KLMAG2GEAC-B031



KLMAG2GEAC-B031
BGA169_18R00X14R00X1R20_2L



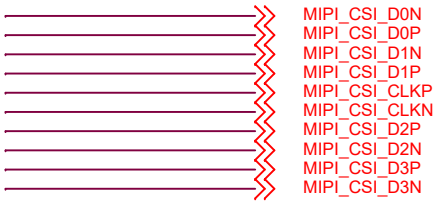


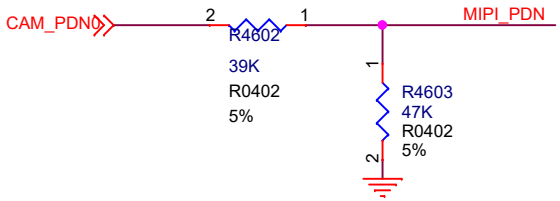
Note:
Short two TP points to Enter Maskrom Mode.

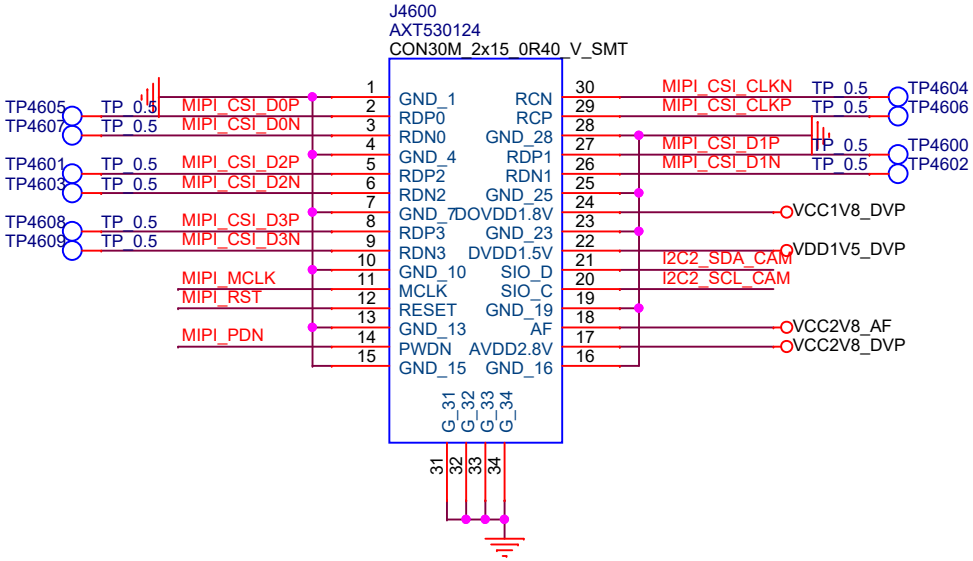
Remind: Refer to the latest AVL for parts selection.

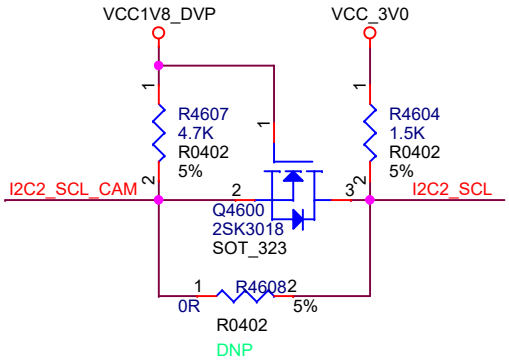
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	41.Flash-EMMC		
Date:	Friday, April 12, 2019	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	21 of 32

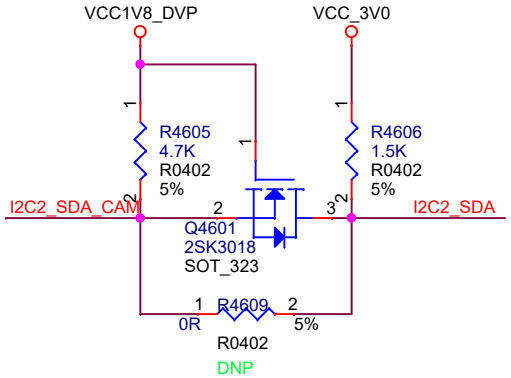
MIPI Camera

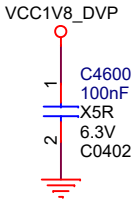


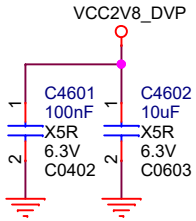


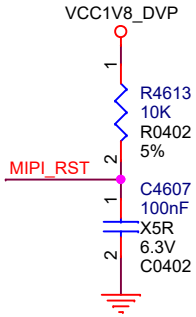


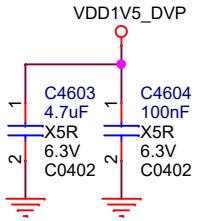


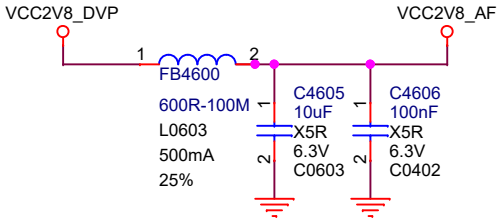








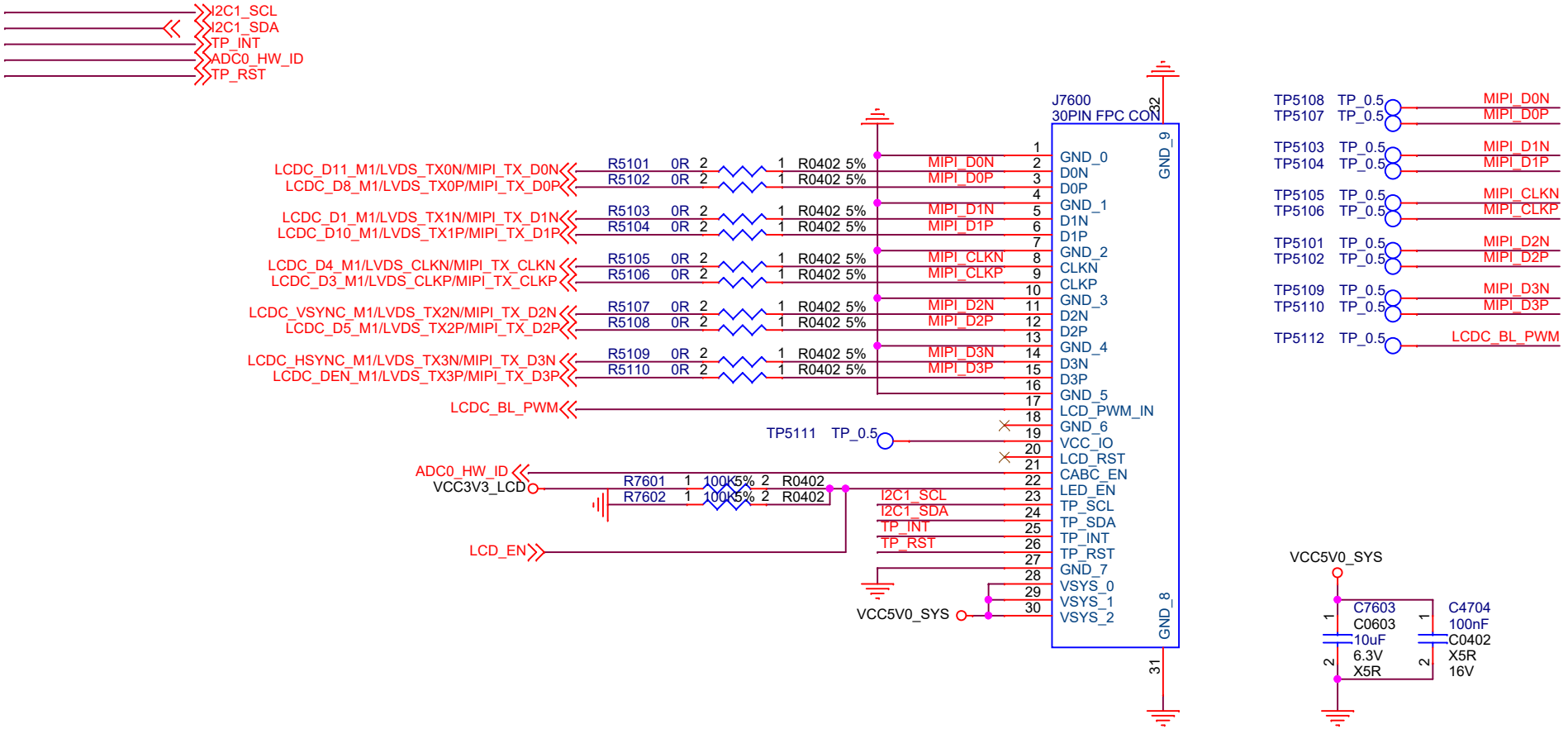




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	46.Camera-MIPI CSI		
Date:	Friday, September 14, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	22 of 32

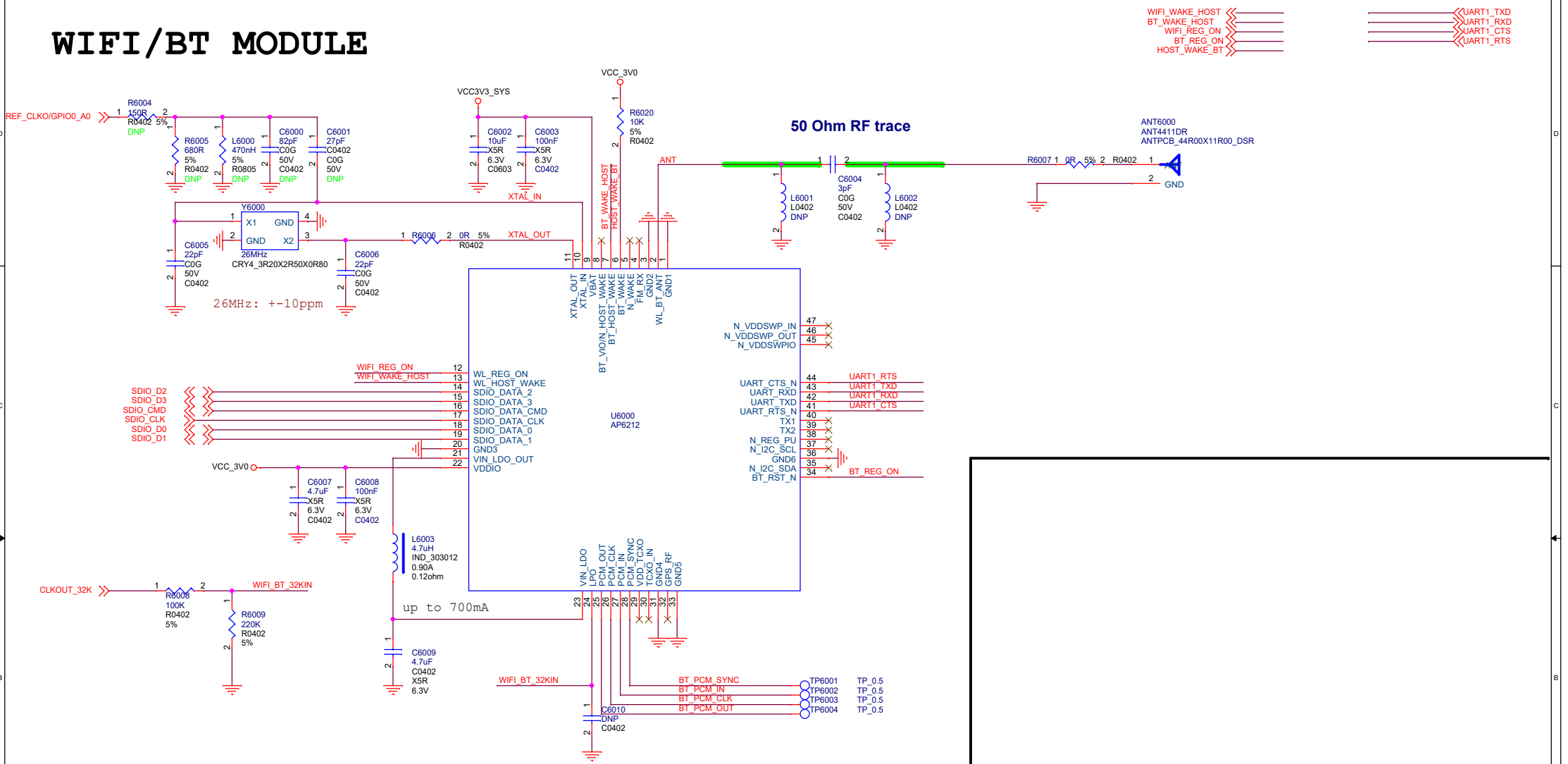
MIPI Panel

Note:
1.Use the MIPI output of RK618,please disconnect the PX30.
2.If need to support of LVDS/MIPI panel and HDMI with dual output same image,
must use the physical cross screen panel,for example 1280x800, not 800x1280

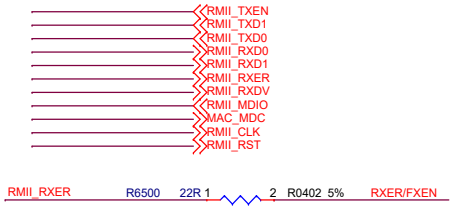


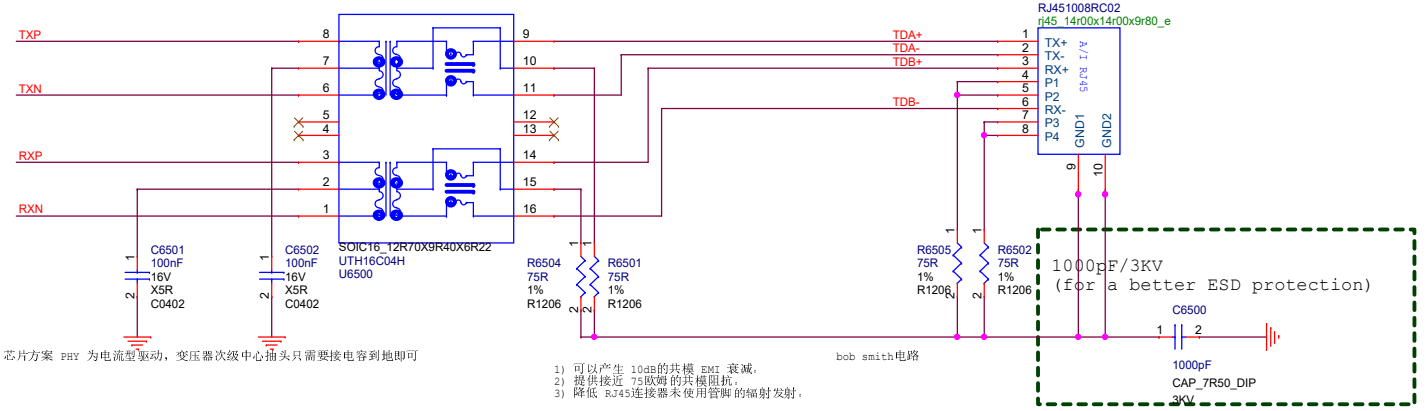
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	52.LCM-MIPI Panel		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	23 of 32

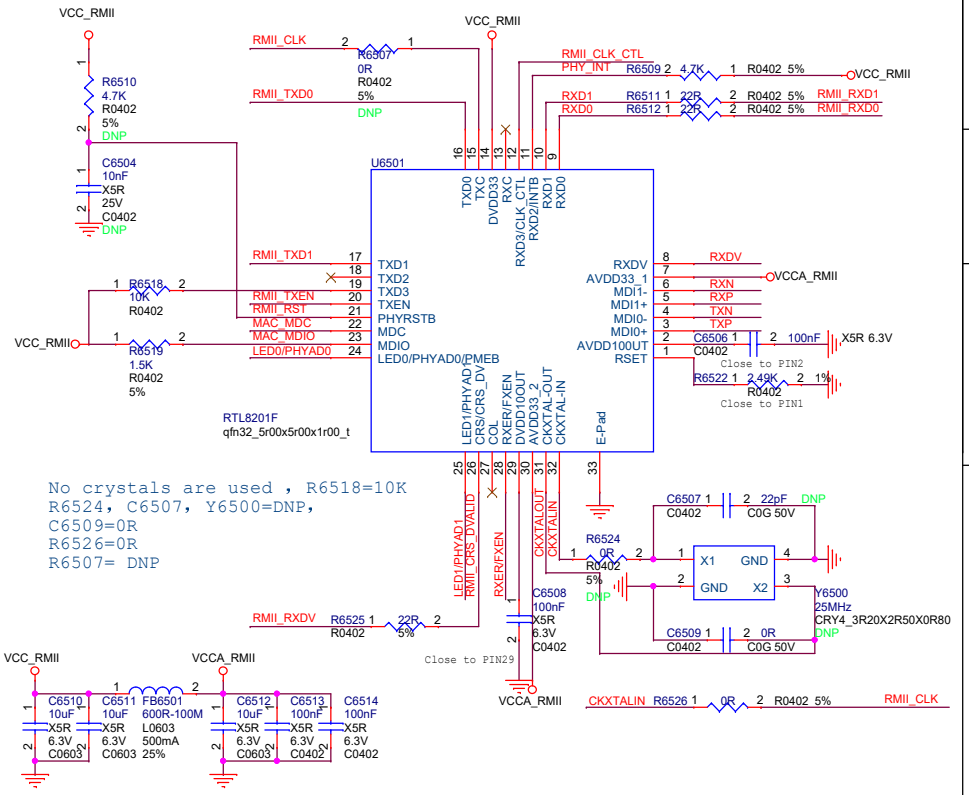
WIFI/BT MODULE



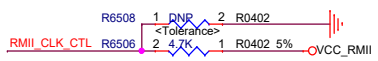
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	60.SDIO WIFI/BT AP6212		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	24 of 32





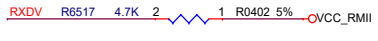


RMII REF_CLK direction



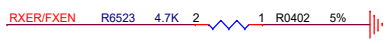
Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

MII/RMII Selection



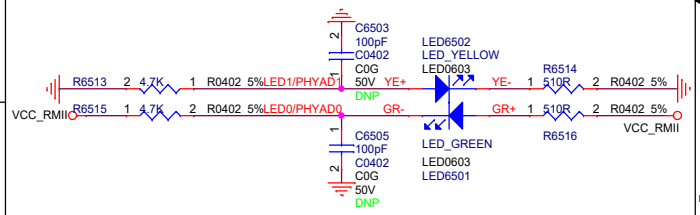
Pull High for RMII mode(default)

UTP / Fiber Selection

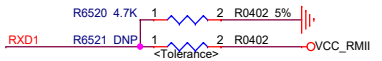


Pull Low for UTP Mode(default)
Pull High for Fiber Mode

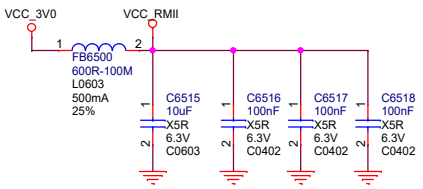
PHY Address/LED



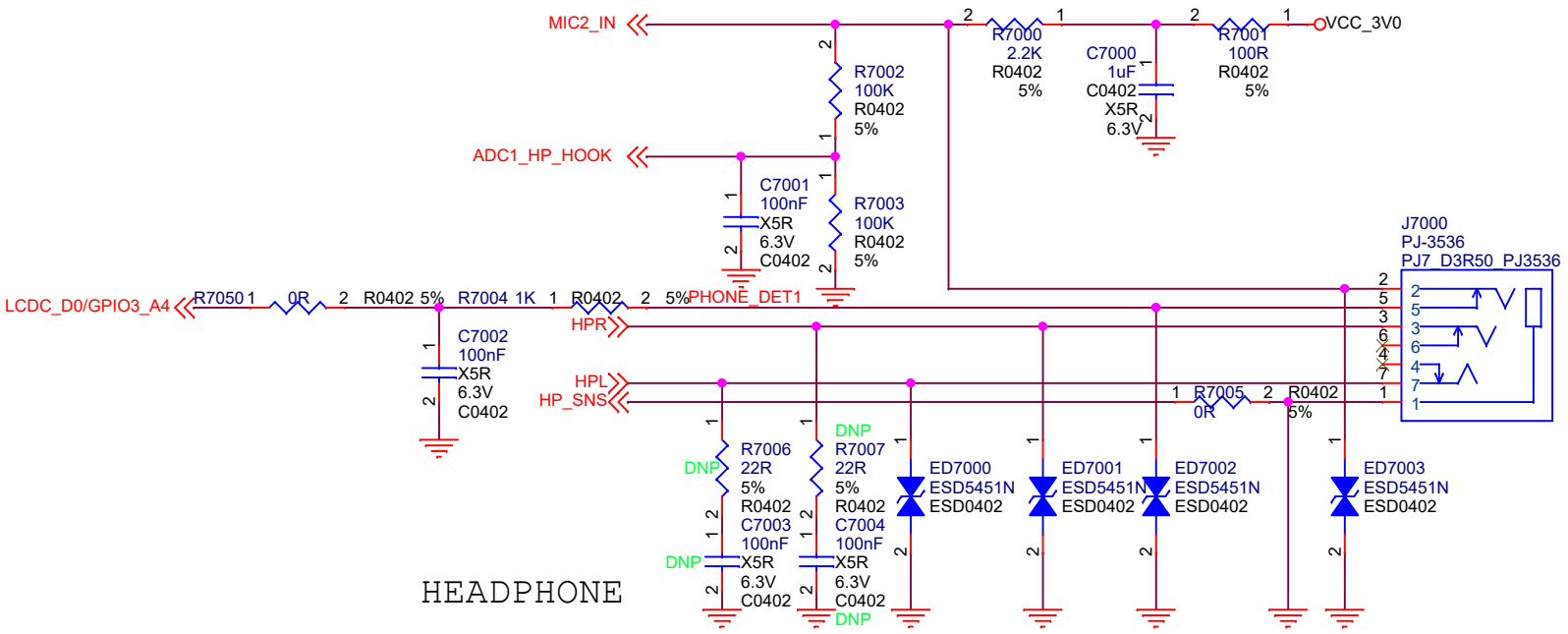
WOL/LED0 Selection

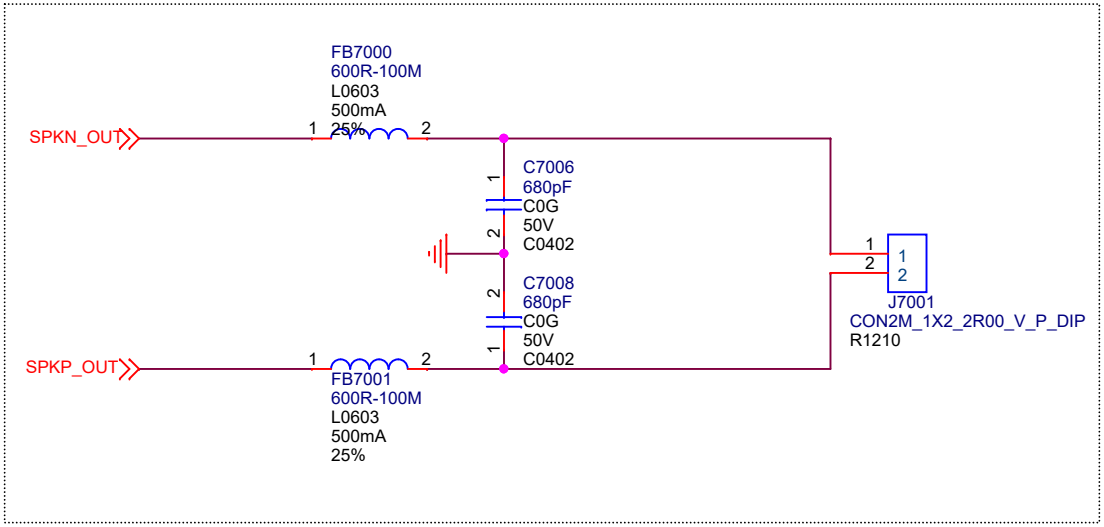


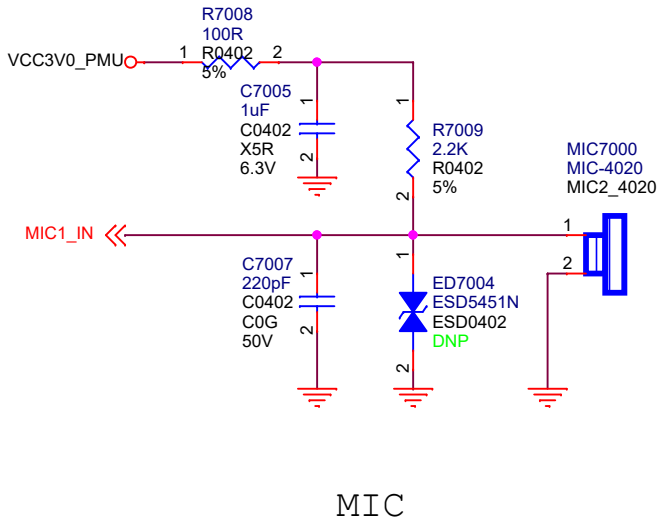
Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	65.RJ45-100M-RTL8201		
Date:	Tuesday, September 25, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	25 of 32





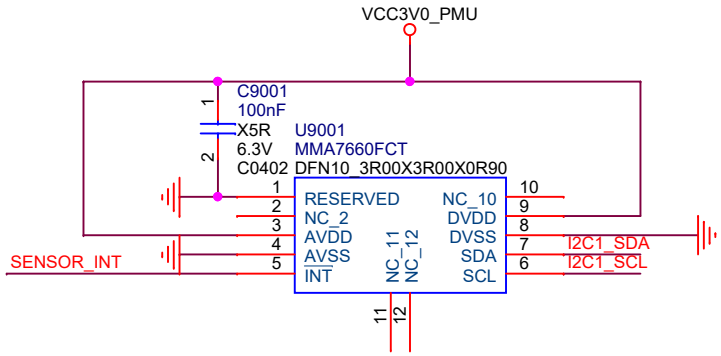


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	70.AUDIO1		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	26 of 32

I2C1_SDA
I2C1_SCL

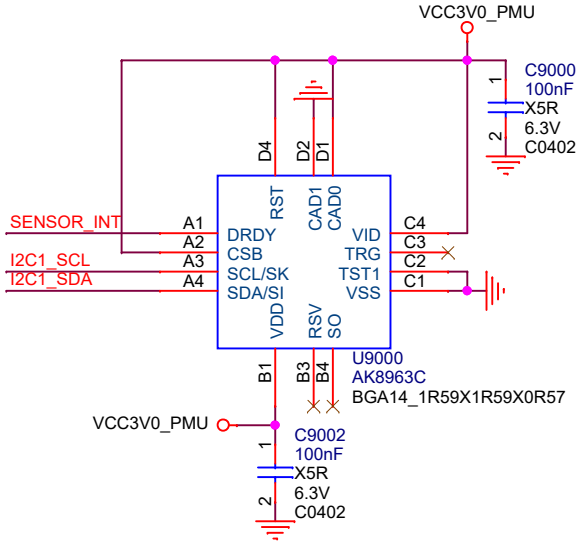
SENSOR_INT

G-sensor



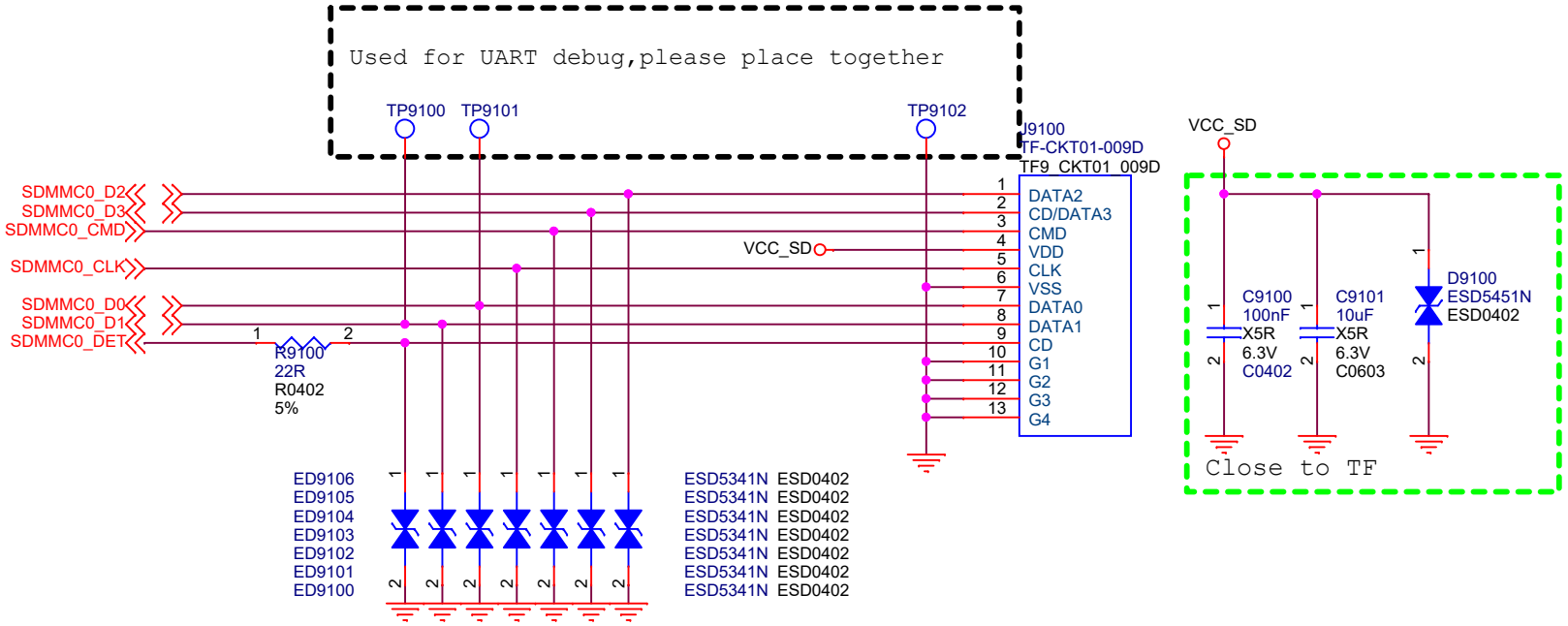
Compass

Note:
The first pin of AK8963C must be place on the lower left corner of PCB.

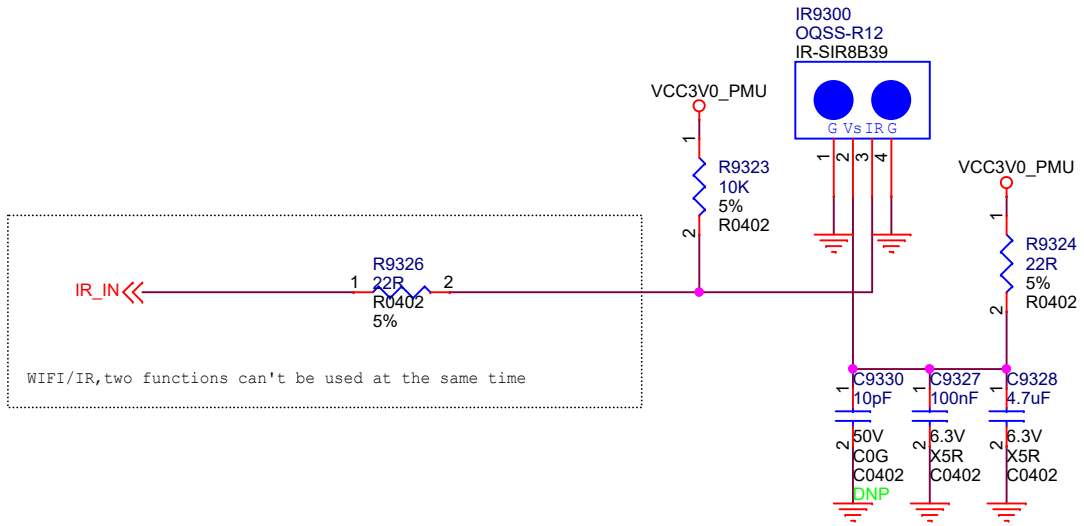


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	90.Sensor		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	27 of 32

TF Card



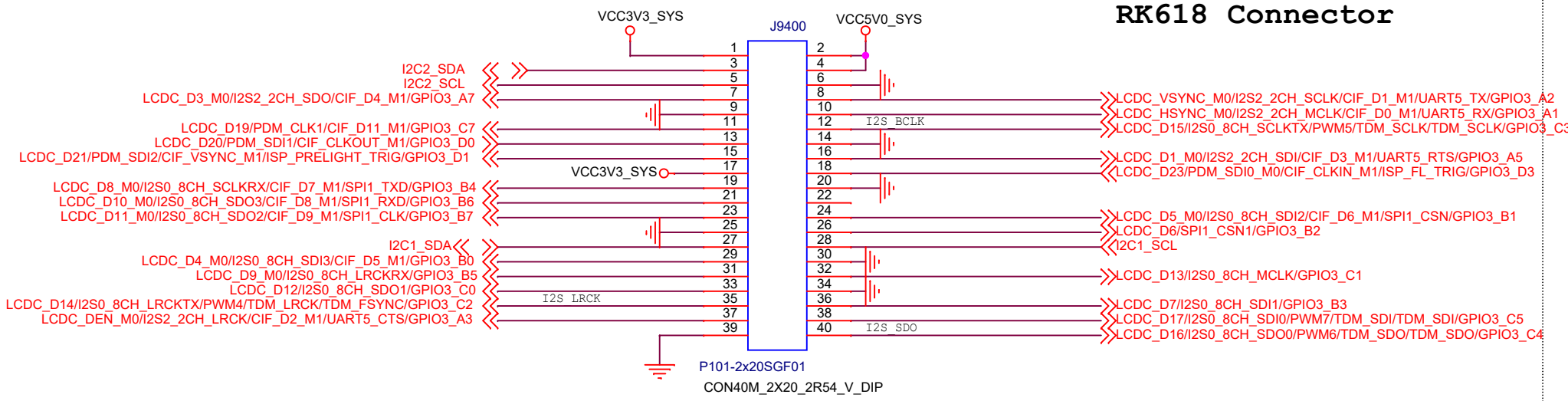
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	91.TF Card		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	28 of 32

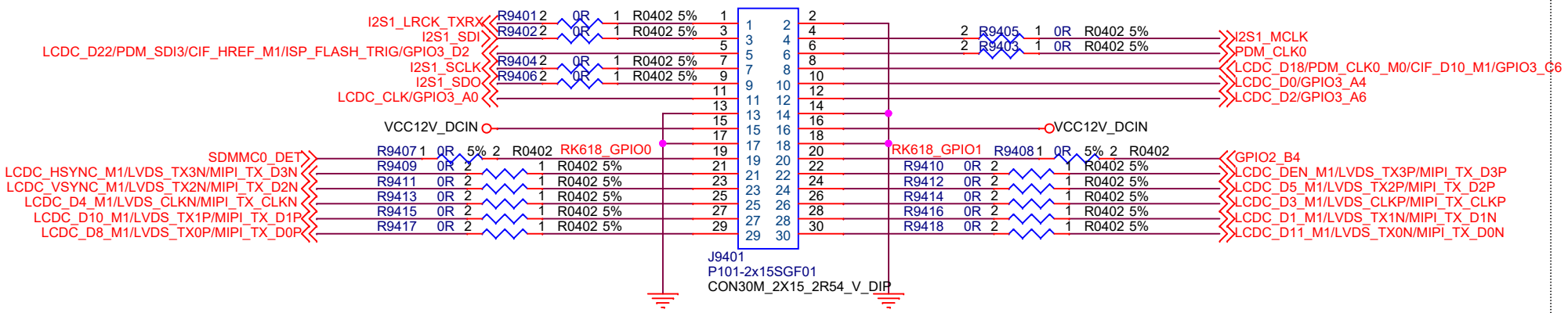


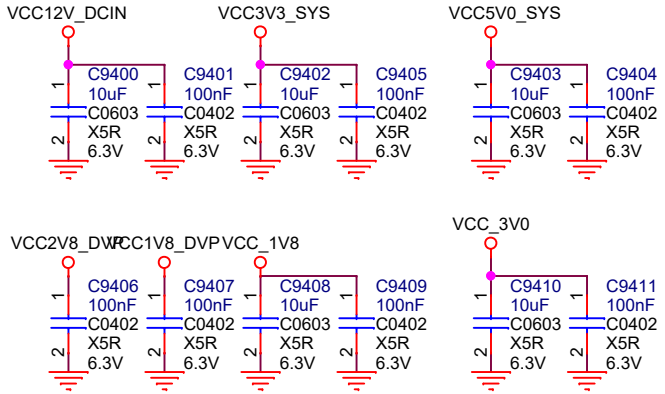
IR Receiver

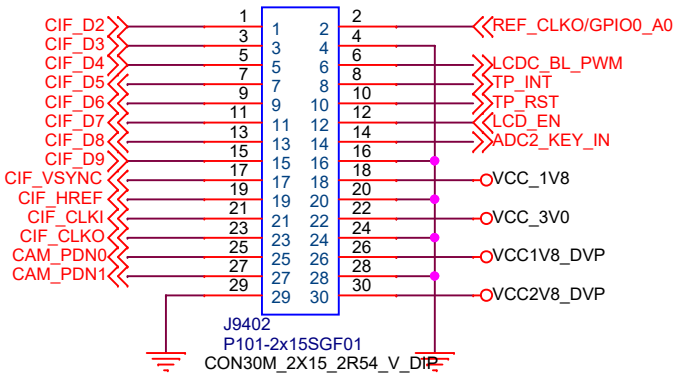
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	93.IR		
Date:	Monday, May 28, 2018	Rev:	V1.0
Designed by:	XIAOHF	Sheet:	29 of 32

RK618 Connector

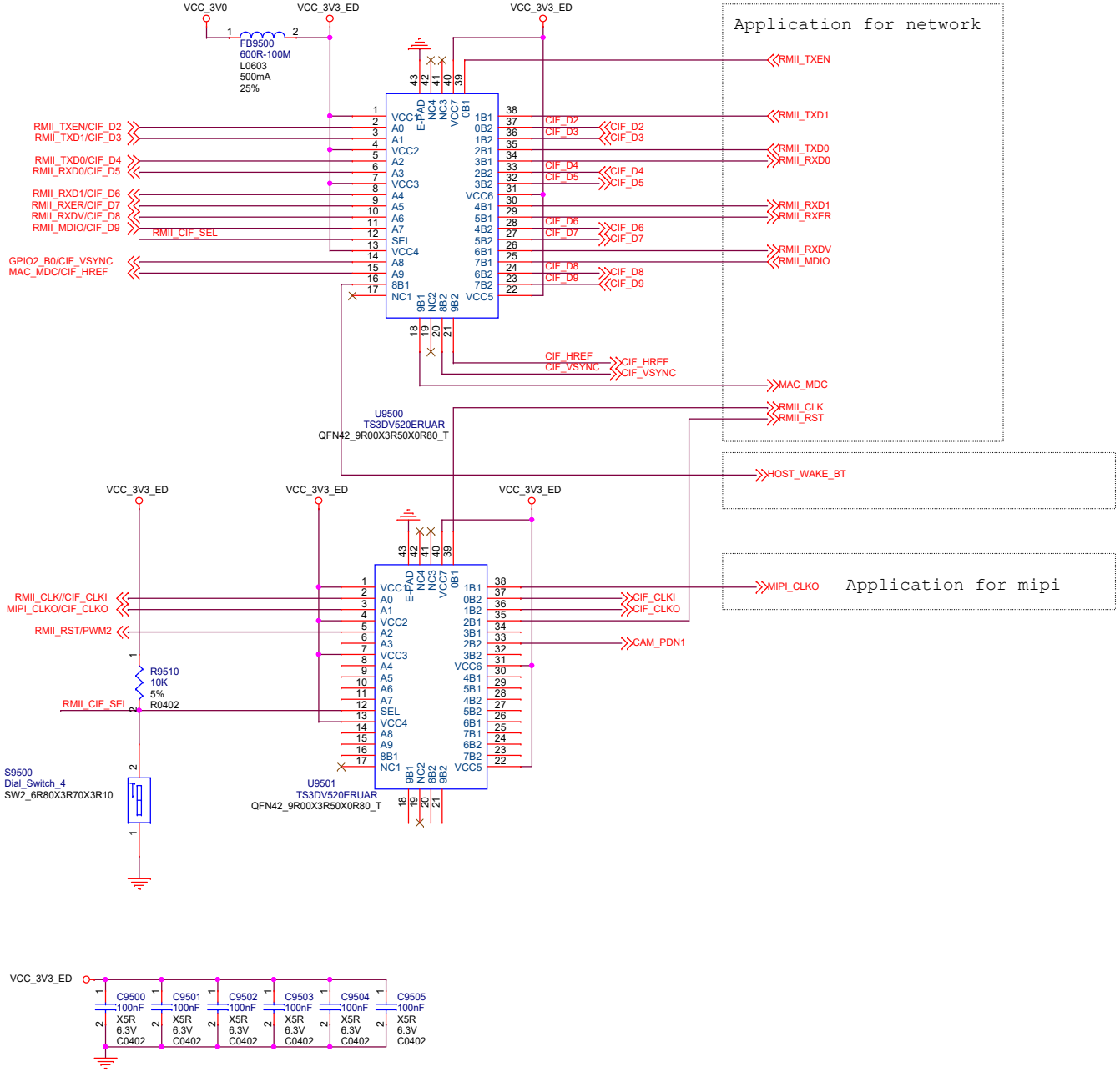




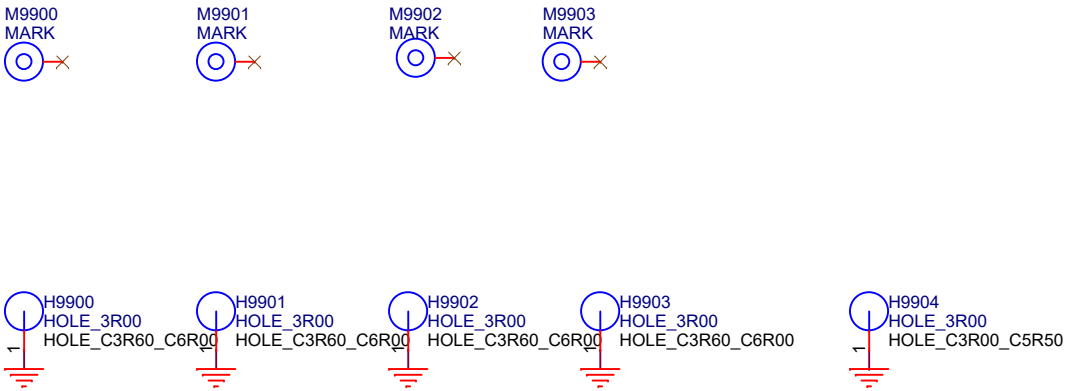




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	94.40PIN/30PIN Connect		
Date:	Monday, May 28, 2018	Rev:	V0.1
Designed by:	XIAOHF	Sheet:	30 of 32

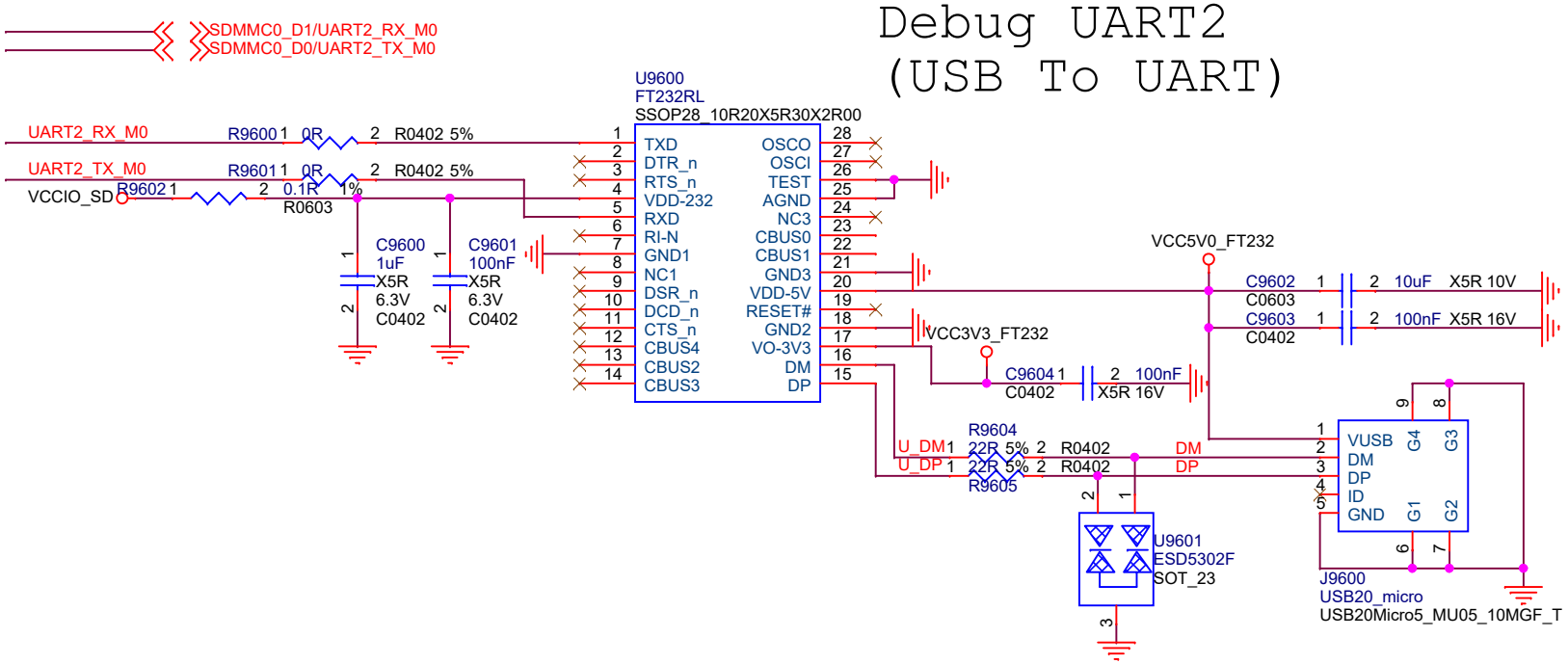


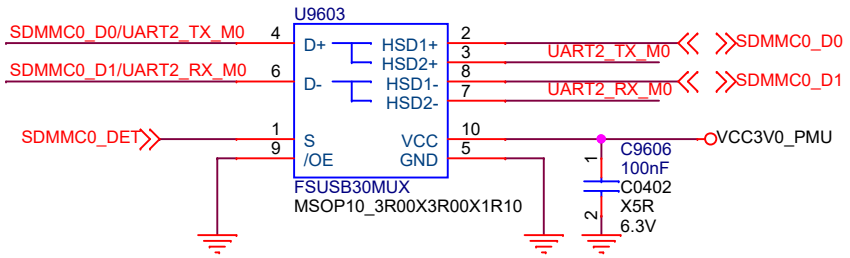
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	95.SWITCH		
Date:	Monday, May 28, 2018	Rev:	V0.1
Designed by:	XIAOHF	Sheet:	31 of 32



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	99.MARK/HOLE		
Date:	Monday, May 28, 2018	Rev:	V0.1
Designed by:	XIAOHF	Sheet:	32 of 32

Debug UART2 (USB To UART)





Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	D+, D– = $HSD1_n$
H	L	D+, D– = $HSD2_n$

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	PX30 MINI EVB		
File:	96.UART Debug		
Date:	Monday, May 28, 2018	Rev:	V0.1
Designed by:	XIAOHF	Sheet:	32 of 35