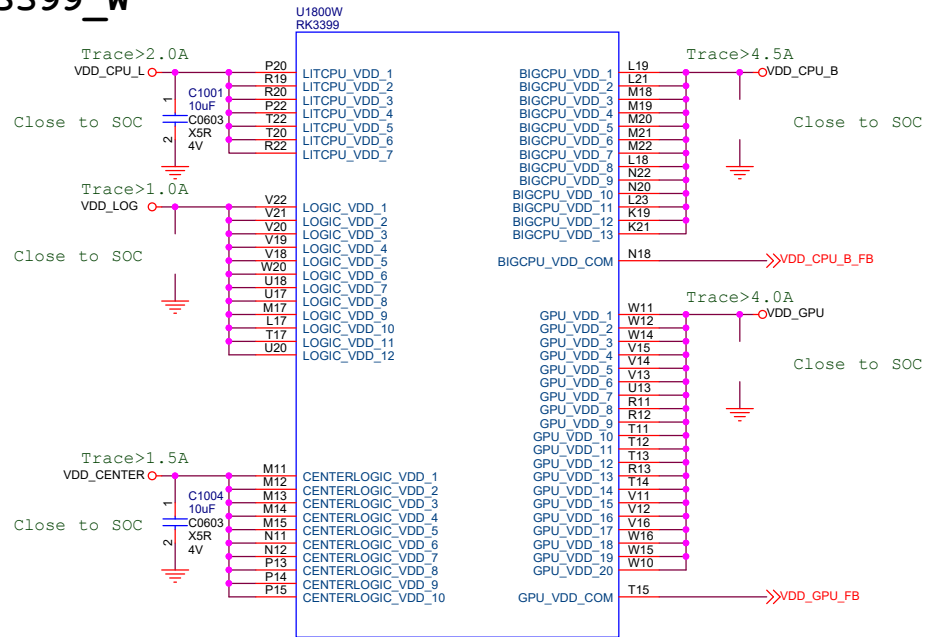


# Revision History

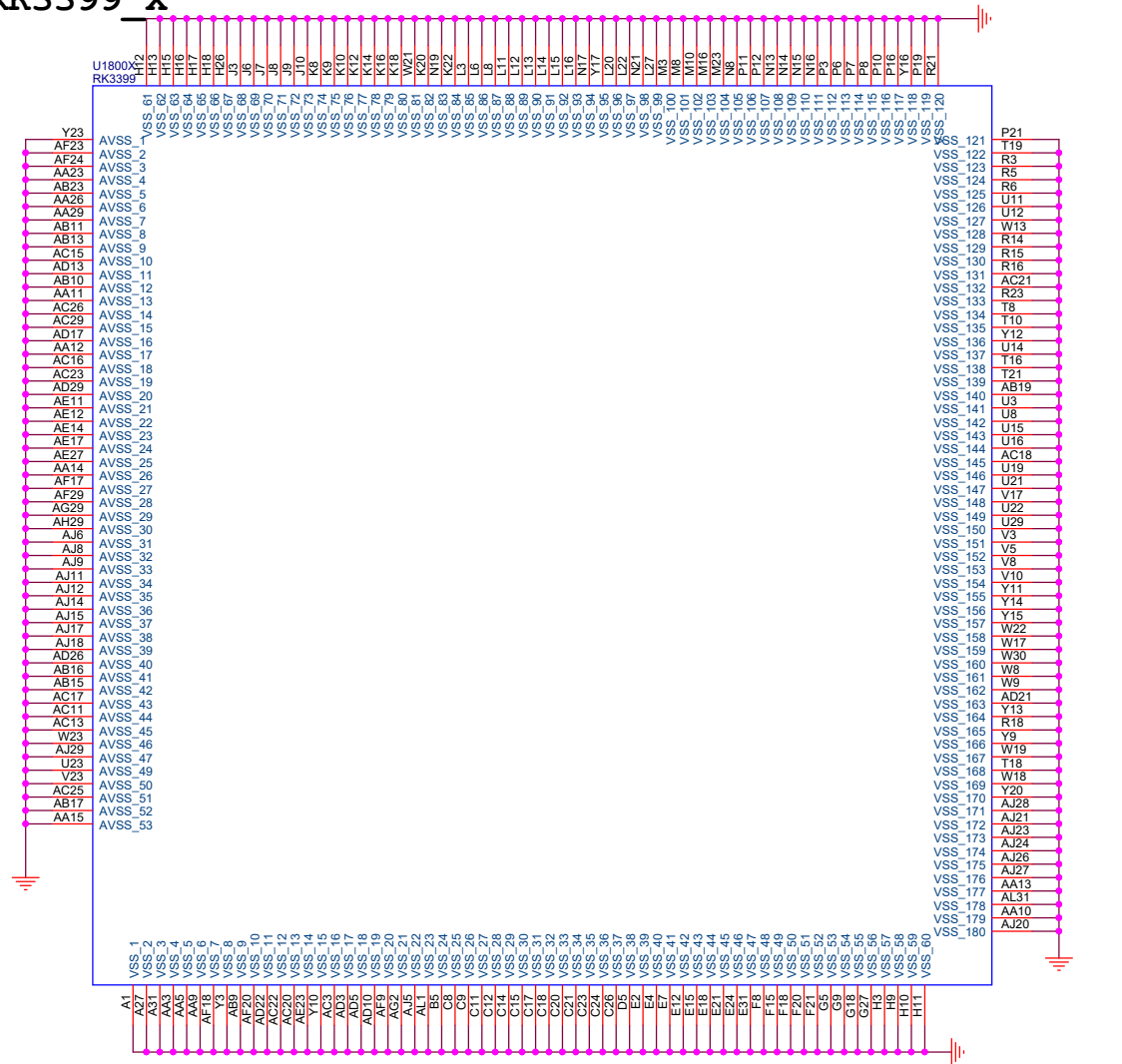
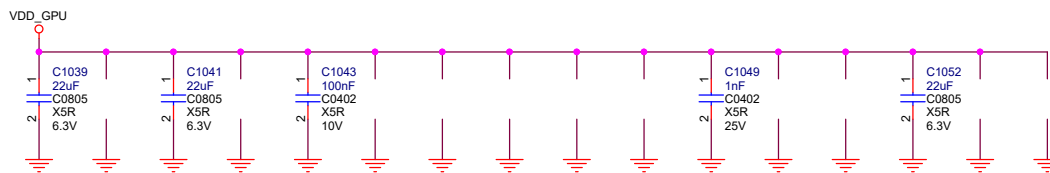
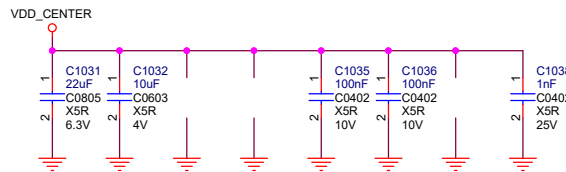
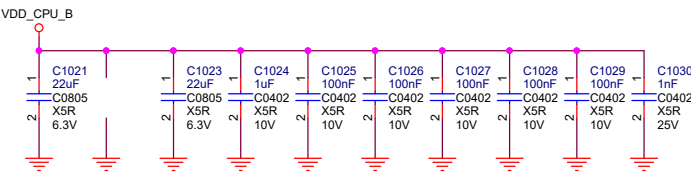
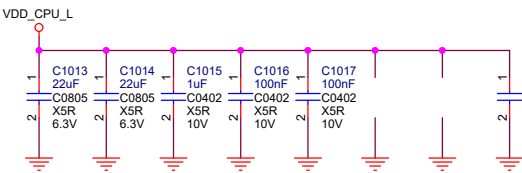
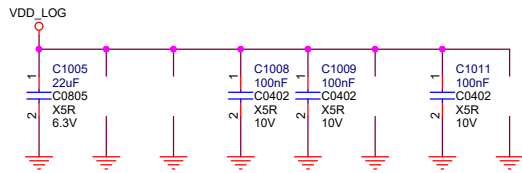
Version	Date	Author	Change Note	Approved
V1.0	2017.01.12	Linus.Lin	First edition	

# RK3399\_W

# RK3399\_X

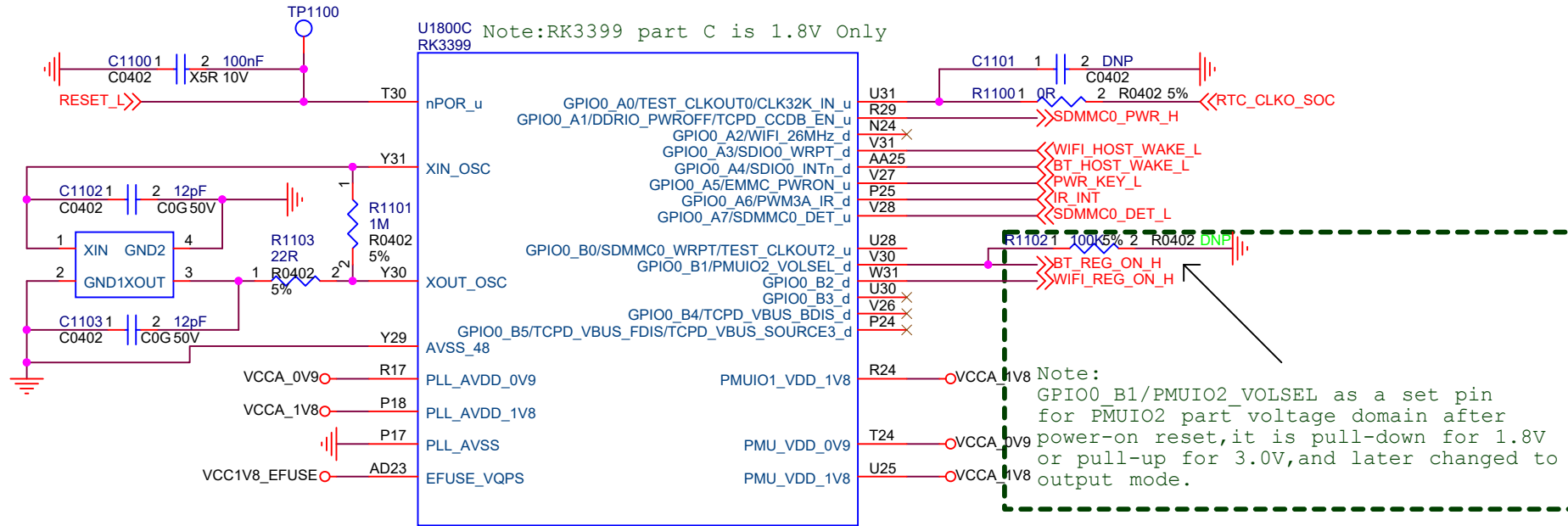


Note: All the Power filter capacitor should be place close to the power pin of RK3399

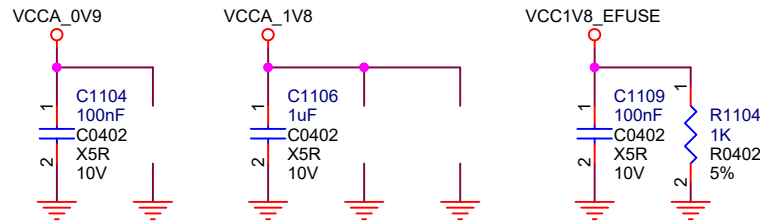


<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	RK3399 Power		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	2 of 33

# RK3399\_C




Y1100  
24MHz  
CRY-D3225

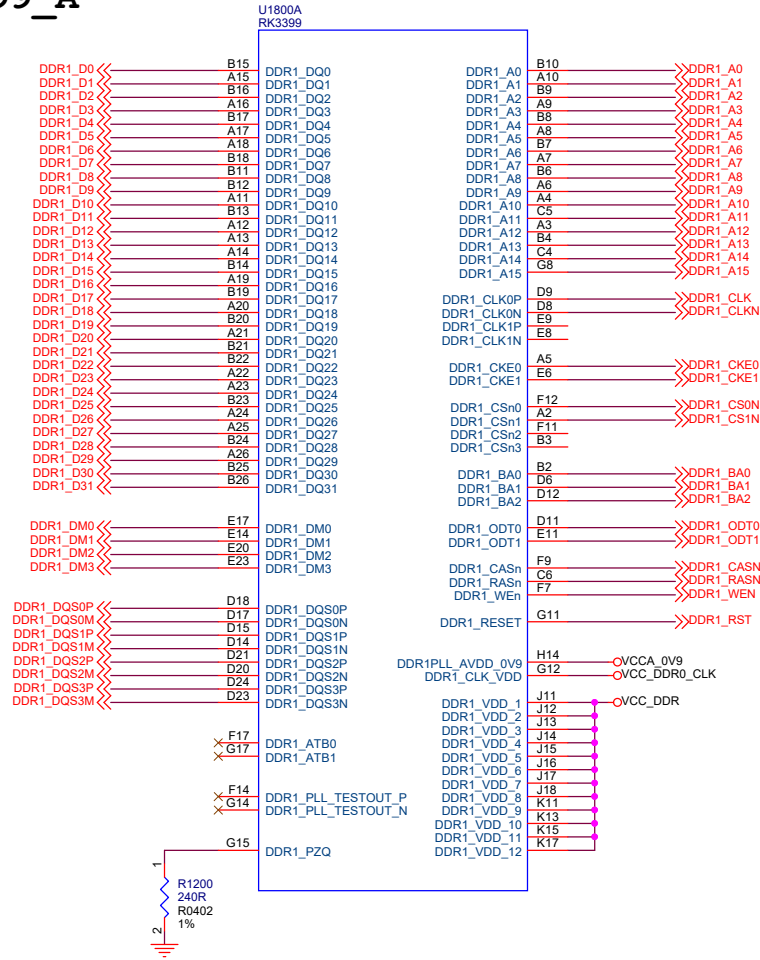


Note:  
R1104 must always be pasted.

Note:All the Power filter capacitor should be place close to the power pin of RK3399

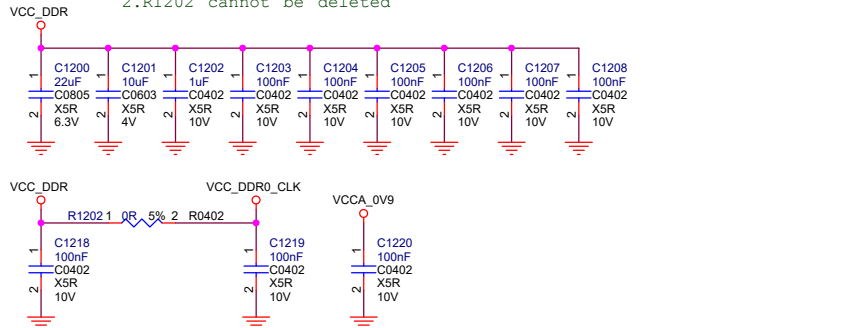
 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	RK3399 PMU Controller
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	3 of 33

# RK3399\_A

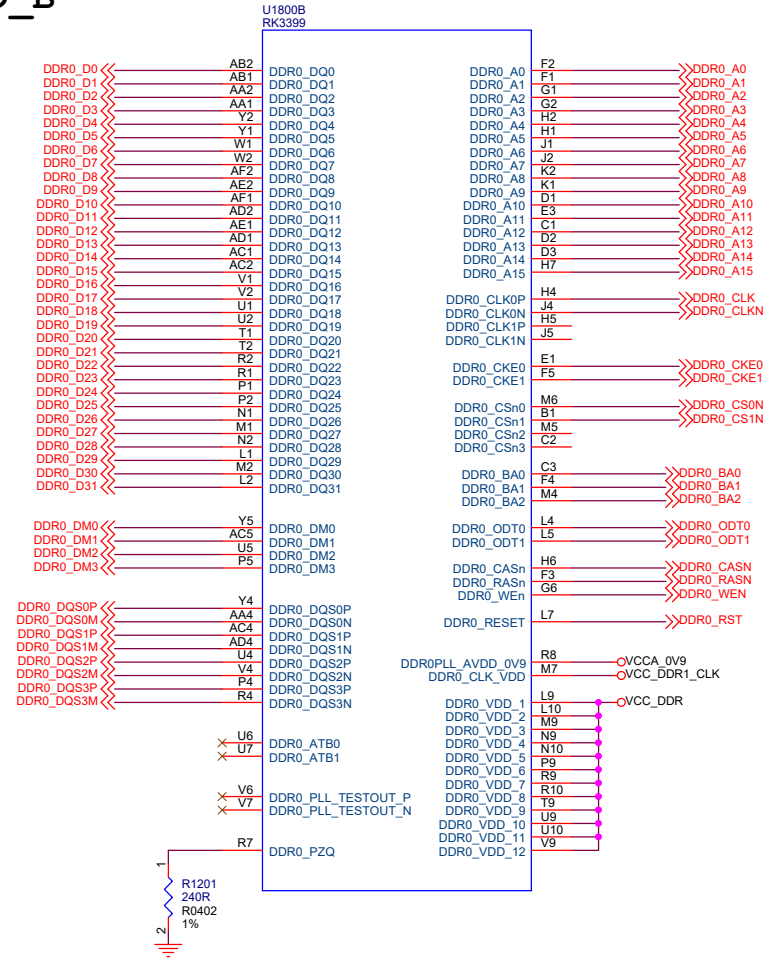


## DDR FILTER

Note:  
1. All the Power filter capacitor should be place close to the power pin of RK3399  
2. R1202 cannot be deleted

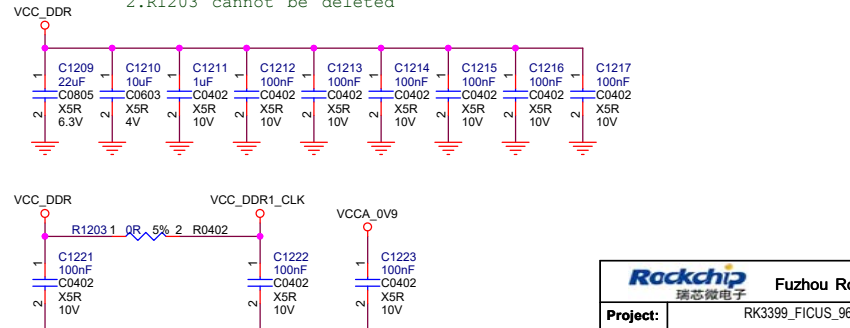


# RK3399\_B



## DDR FILTER

Note:  
1. All the Power filter capacitor should be place close to the power pin of RK3399  
2. R1203 cannot be deleted

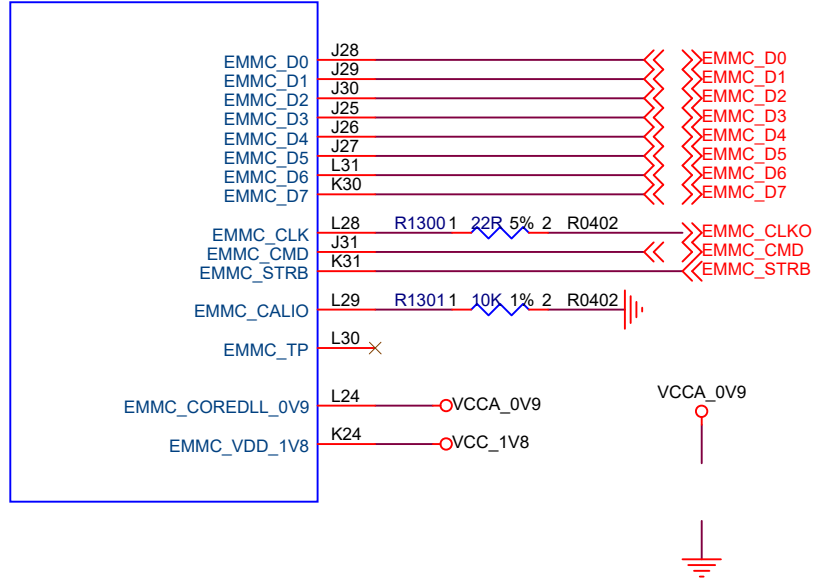


**Rockchip** Fuzhou Rockchip Electronics  
瑞芯微电子

Project:	RK3399_FICUS_96BOARDS		
File:	RK3399 DDR Controller		
Date:	Friday, July 06, 2018	Rev:	V1.0
Designed by:	Linus	Sheet:	4 of 33

# RK3399\_H

U1800H  
RK3399



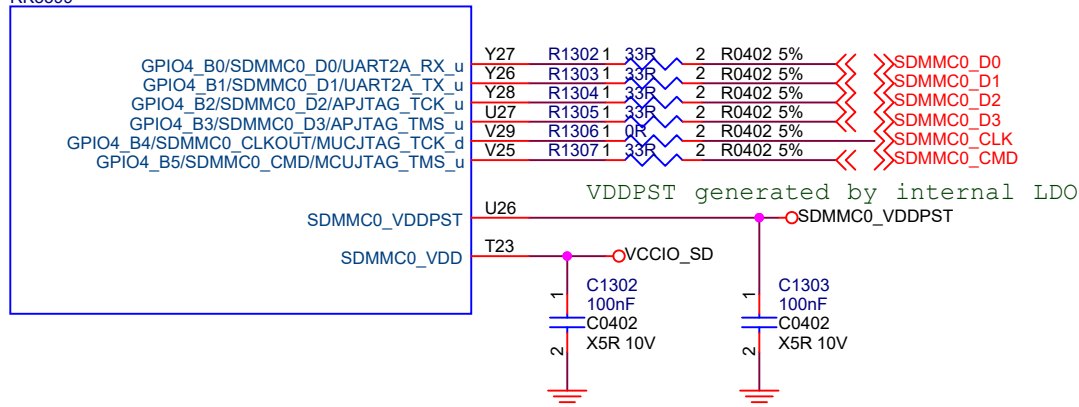
EMMC design rule:

- 1.Data[0:3] ,CMD and Strobe lines routing parallel as a group, and be isolated with other signal by GND line,the skew between group is less than 200mil;
- 2.Clk should be isolated with other signal by GND line;The skew between data signal is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;
- 6.R1300 should be place close to RK3399;

Note:All the Power filter capacitor should be place close to the power pin of RK3399

# RK3399\_F

U1800F  
RK3399

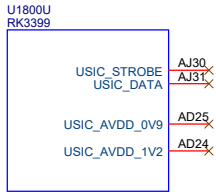


SDMMC design rule:

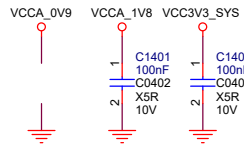
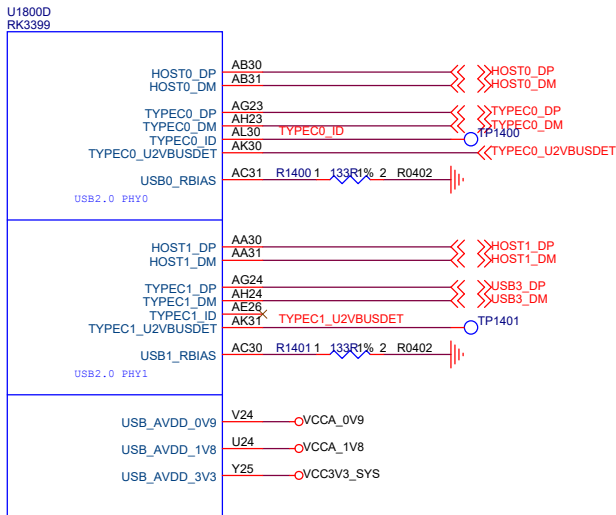
- 1.Data[0:3] and CMD lines routing parallel as a group, and be isolated with other signal by GND line,the skew between group is less than 200mil;
- 2.Clk should be isolated with other signal by GND line;The skew between data signal is less than 20ps;
- 3.Max trace length < 3.93 inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	RK3399_FLASH/SDMMC Controlle		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	5 of 33

# RK3399\_U



# RK3399\_D

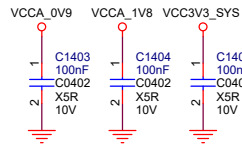
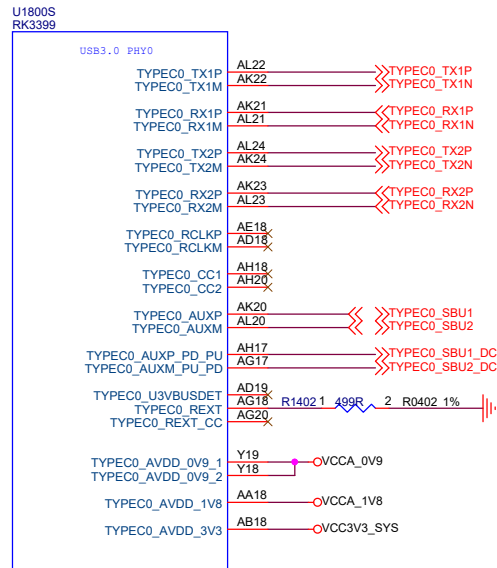


Note: All the Power filter capacitor should be place close to the power pin of RK3399

USB2.0 design rule:

1. Max intra-pair skew < 4 ps;
2. Max trace length < 6 inchs;
3. Max allowed via < 6;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

# RK3399\_S

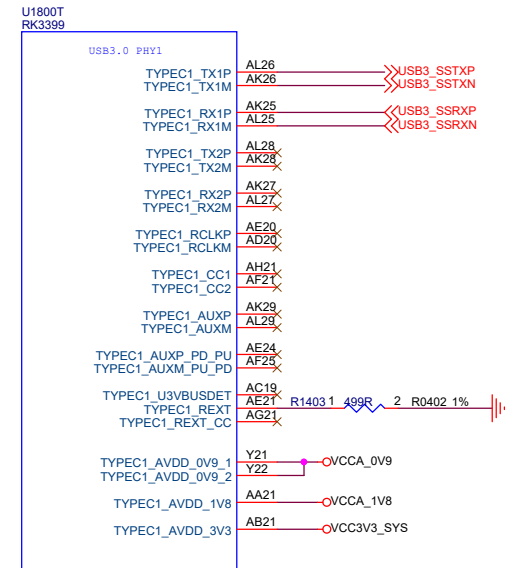


Note: All the Power filter capacitor should be place close to the power pin of RK3399

USB3.0 design rule:

1. Max intra-pair skew < 4 ps;
2. Max length skew between TX and RX < 1.6 ns;
3. Max trace length < 6 inchs;
4. Max allowed via < 4;
5. Trace impedance 90ohm+/-10%;
6. The distance between other signals follows the 3W rule;

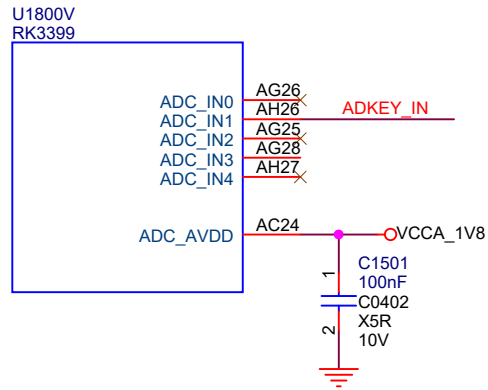
# RK3399\_T



- DP design rule:
1. Max intra-pair skew < 4 ps;
  2. Max trace length < 6 inchs;
  3. Max allowed via < 4;
  4. Trace impedance 90ohm+/-10%;
  5. The distance between other signals follows the 3W rule;

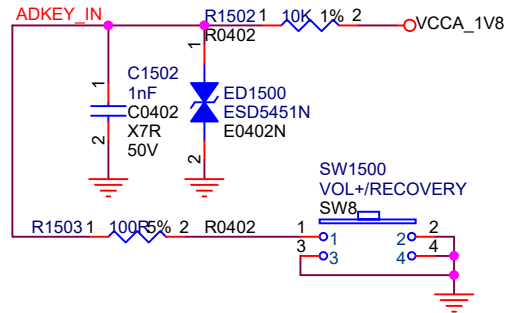
<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	RK3399 USB/USIC Controller		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	6 of 33

# RK3399\_V




Note: All the Power filter capacitor should be place close to the power pin of RK3399

# KEY

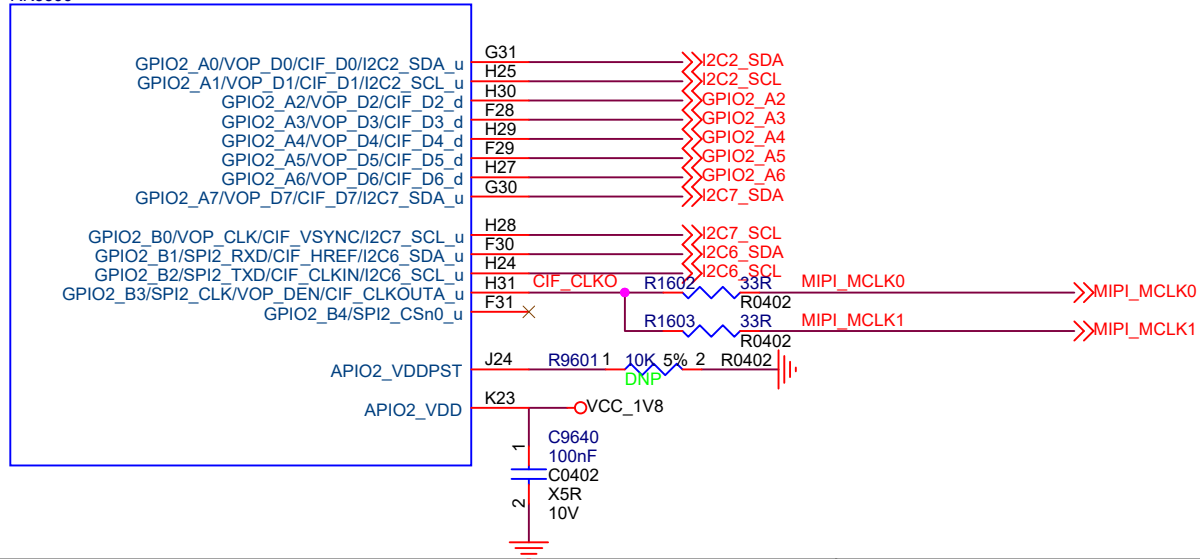


Note:  
 1. If ADKEY\_IN=0V at boot-time, then system will enter into Recovery mode.  
 2. R1503, SW1500, ED1500 do not paster in Mass Production.

 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	RK3399 SAR-ADC/Key
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	7 of 33

# RK3399\_L

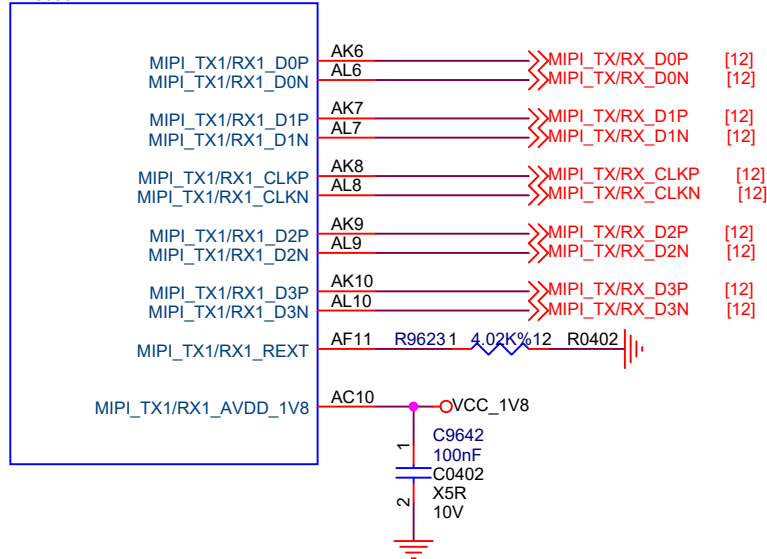
U1800L  
RK3399



- [26] MIPI design rule:
1. Max intra-pair skew < 4 ps;
  2. Max length skew between clk and data < 7ps;
  3. Max trace length < 7.2 inches;
  4. Max allowed via < 4;
  5. Trace impedance 100ohm+/-10%;
  6. The distance between other signals follows the 3W rule;

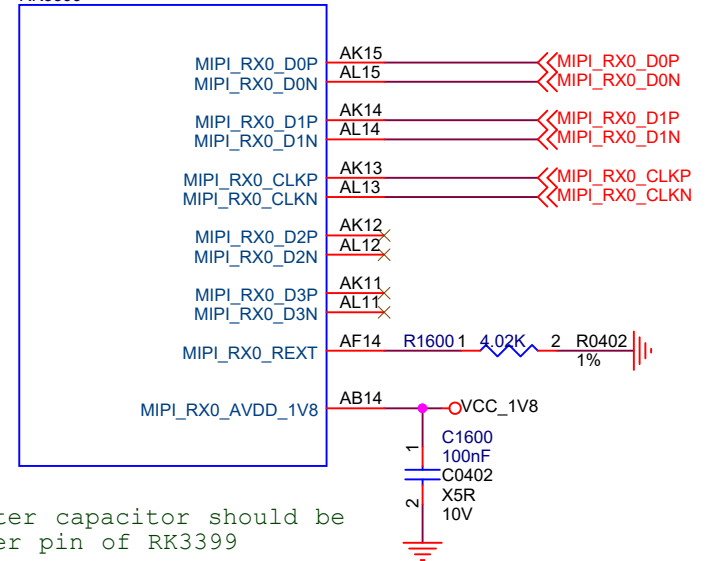
# RK3399\_P

U1800P  
RK3399




# RK3399\_R

U1800R  
RK3399



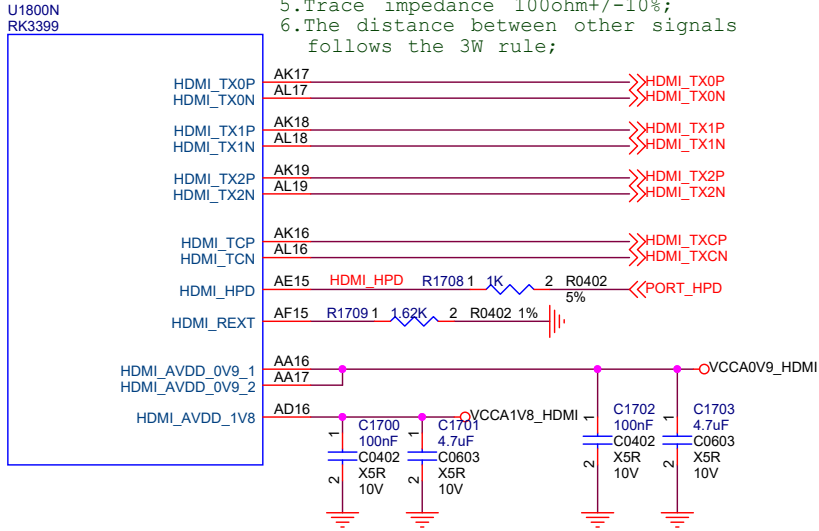
Note: All the Power filter capacitor should be place close to the power pin of RK3399

 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	RK3399 DVP Interface
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	8 of 33



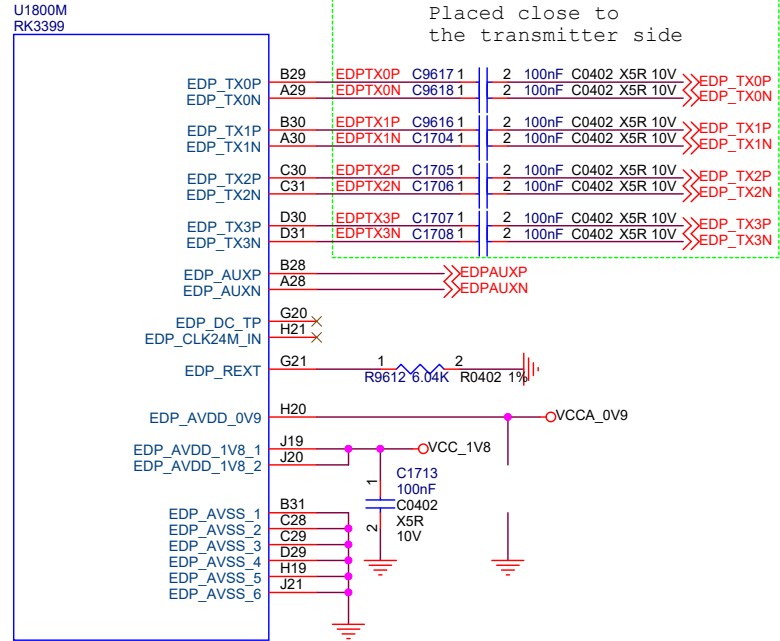
# RK3399\_N

HDMI design rule:  
 1.Max intra-pair skew < 4 ps;  
 2.Max length skew between clk and data < 80 ps;  
 3.Max trace length < 9.8 inchs;  
 4.Max allowed via < 4;  
 5.Trace impedance 100ohm+/-10%;  
 6.The distance between other signals follows the 3W rule;



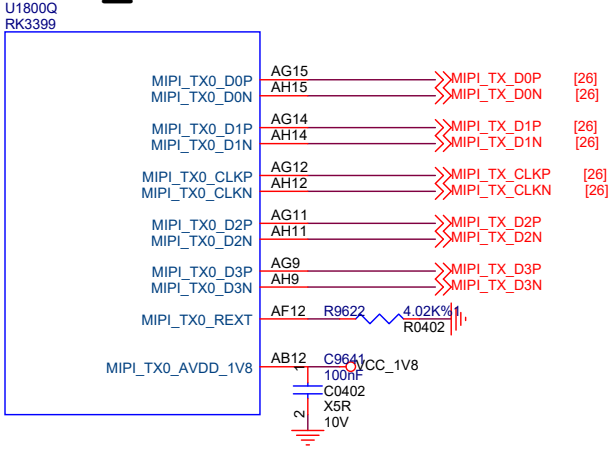
Note:All the Power filter capacitor should be place close to the power pin of RK3399

# RK3399\_M



eDP design rule:  
 1.Max intra-pair skew < 4 ps;  
 2.Max trace length < 6 inchs;  
 3.Max allowed via < 4;  
 4.Trace impedance 90ohm+/-10%;  
 5.The distance between other signals follows the 3W rule;

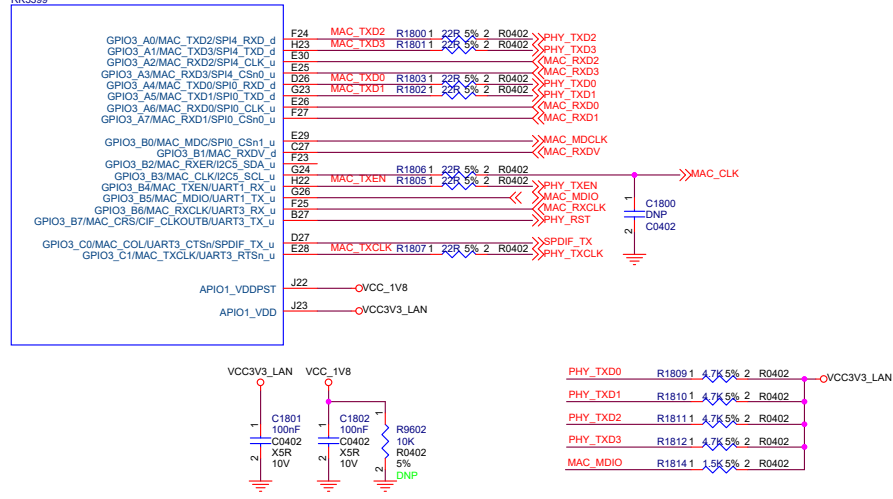
# RK3399\_Q



<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	RK3399 Display Interface		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	9 of 33

# RK3399\_I

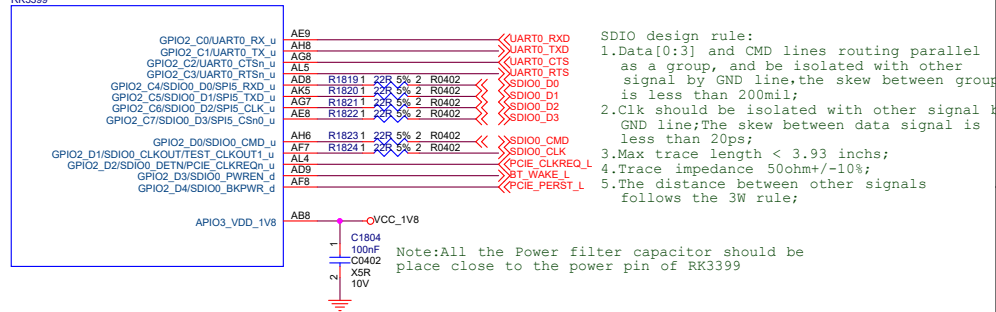
U1800I Note:RK3399 part I is 3.3V only



Note:All the Power filter capacitor should be place close to the power pin of RK3399

# RK3399\_G

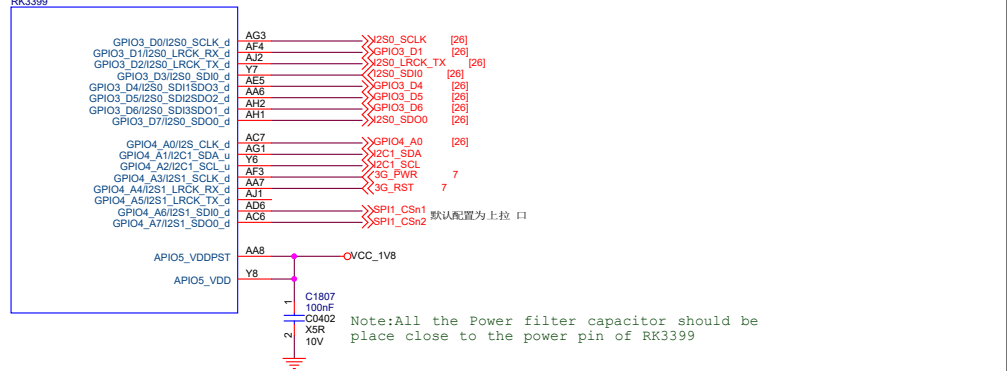
U1800G Note:RK3399 part G is 1.8V only



Note:All the Power filter capacitor should be place close to the power pin of RK3399

# RK3399\_J

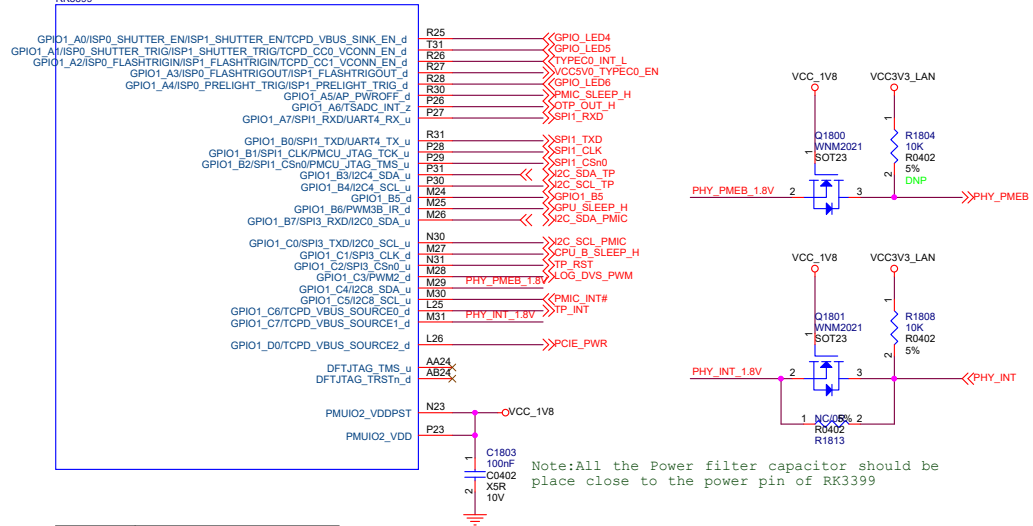
U1800J Note:RK3399 part J is 1.8V/3.0V mode



Note:All the Power filter capacitor should be place close to the power pin of RK3399

# RK3399\_E

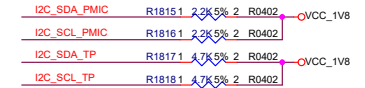
U1800E Note:RK3399 part E is 1.8V/3.0V mode



Note:All the Power filter capacitor should be place close to the power pin of RK3399

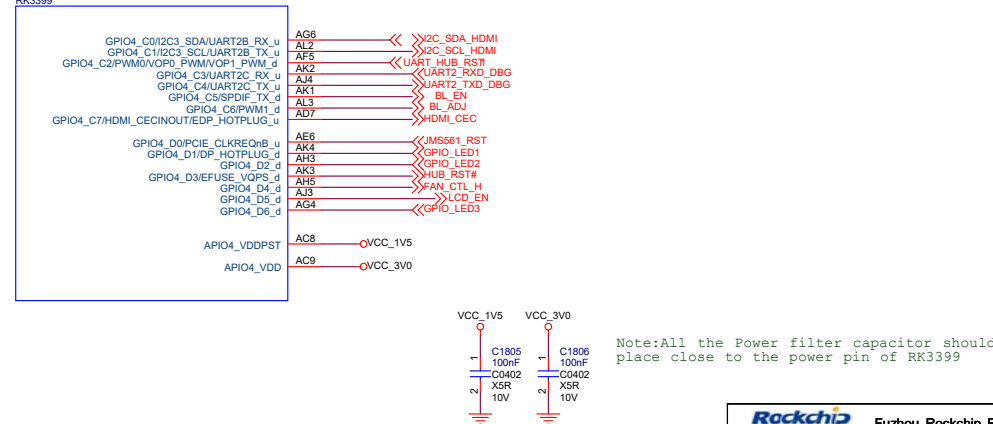
1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
other	3.0V mode:VDDPST=1.8V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V

Note:PMUIO2 part voltage support 1.8V and 3.0V mode, software config should match with hardware design.



# RK3399\_K

U1800K Note:RK3399 part K is 1.8V/3.0V mode

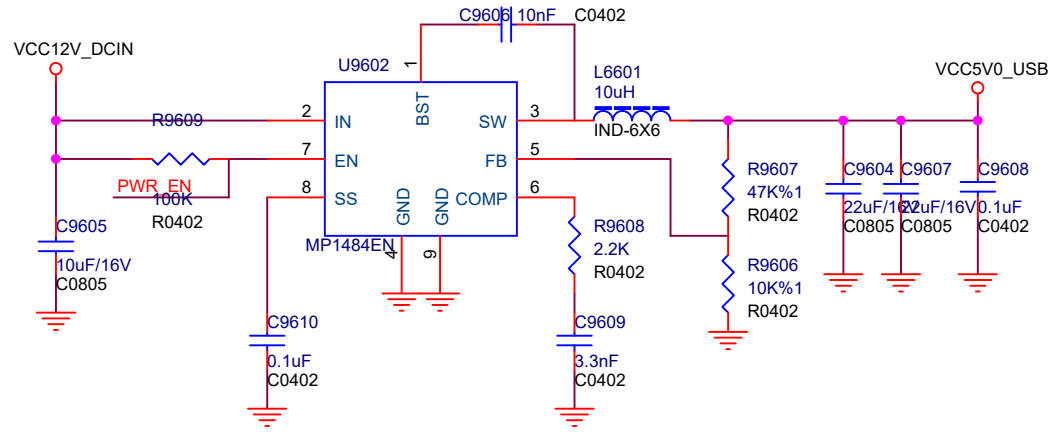
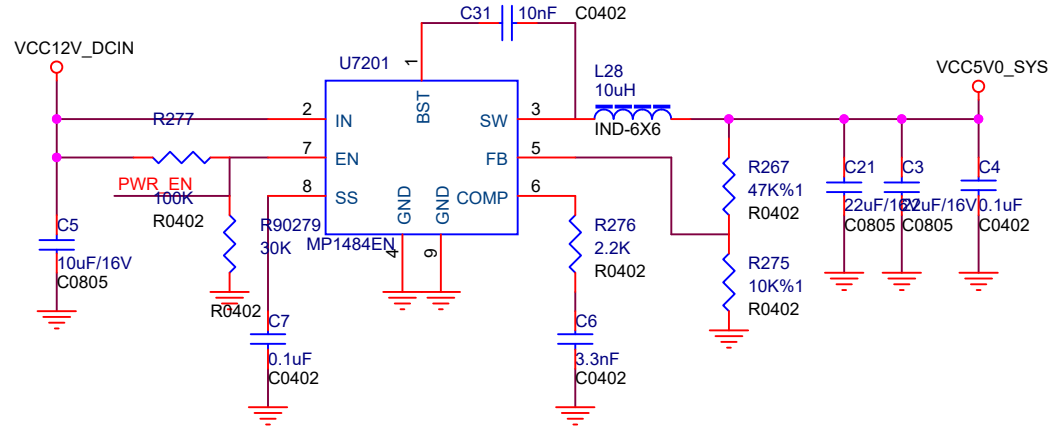
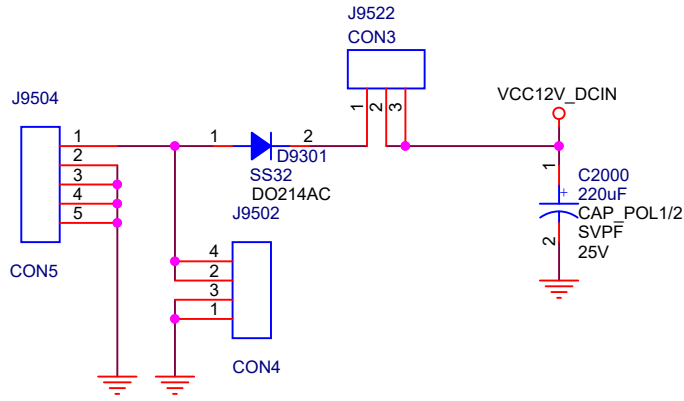



Note:All the Power filter capacitor should be place close to the power pin of RK3399

		<b>Fuzhou Rockchip Electronics</b>	
Project:	RK3399_FICUS_96BOARDS		
File:	RK3399_GPIO		
Date:	Friday, July 06, 2018	Rev:	V1.0
Designed by:	Linux	Sheet:	10 of 38

# DC IN & SYSTEM Power

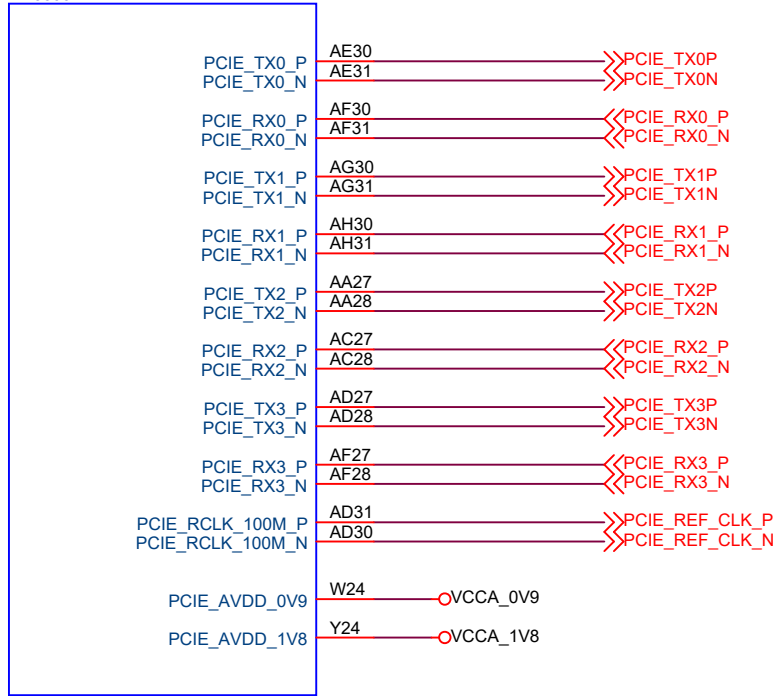
→ PWR\_EN



 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子			
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	Power-DC IN		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	11 of 33

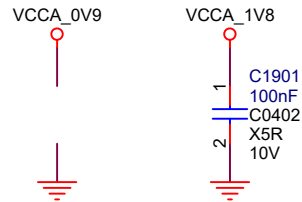
# RK3399\_O

U18000  
RK3399




## PCIE design rule:

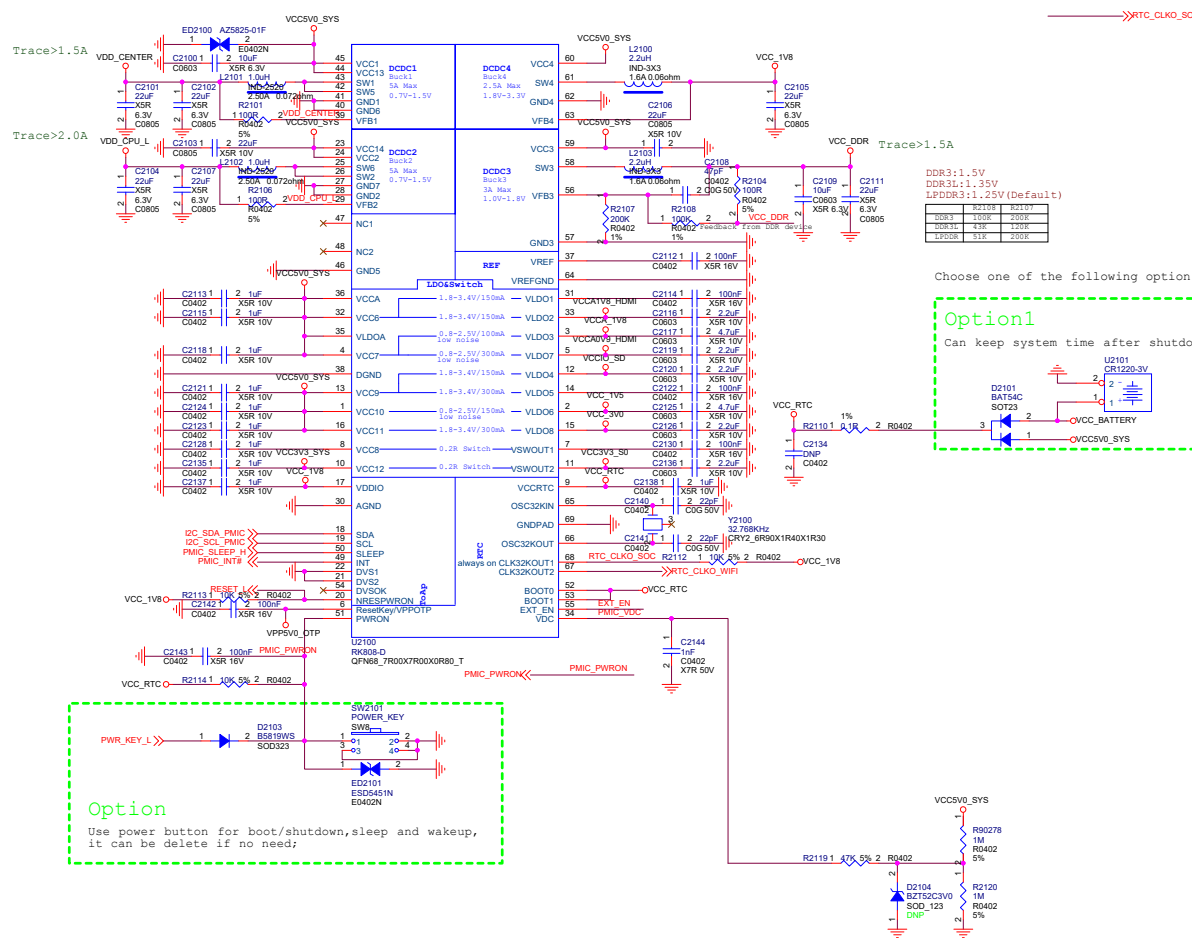
1. Max intra-pair skew < 4ps;
2. Max inter-pair skew < 1.6 ns;
3. Max trace length < 14 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. The distance between other signals follows the 3W rule;



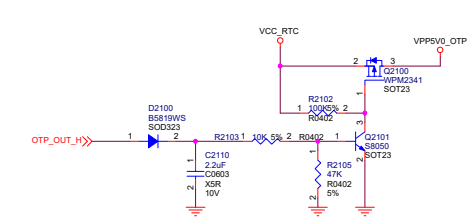
Note: All the Power filter capacitor should be place close to the power pin of RK3399

 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	RK3399_PCIE
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	12 of 33

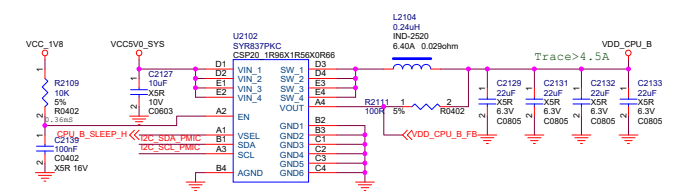
# PMIC RK808-D



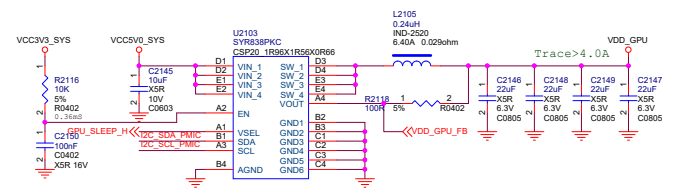
# Over-temperature Protection & RESET



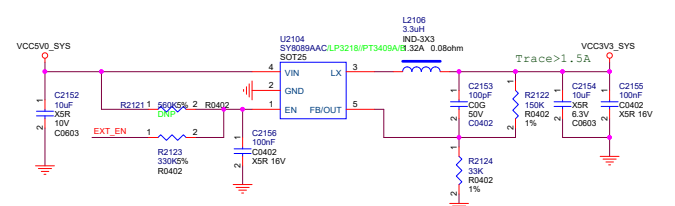
# VDD\_CPU\_B Power



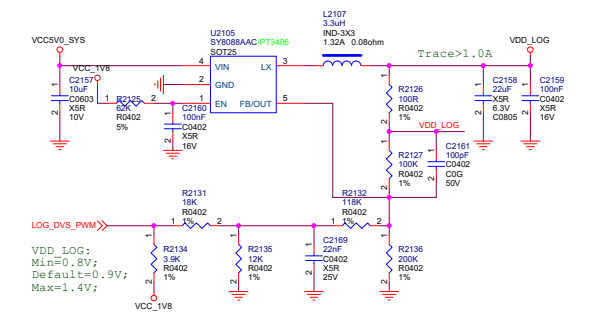
# VDD\_GPU Power



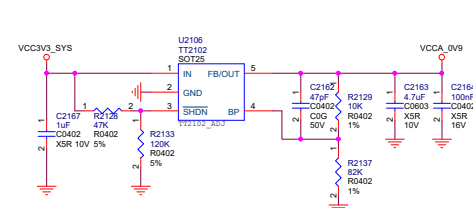
# VCC3V3\_SYS Power



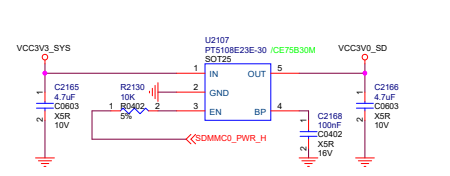
# VDD\_LOG Power

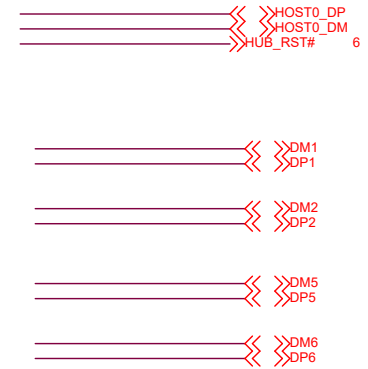
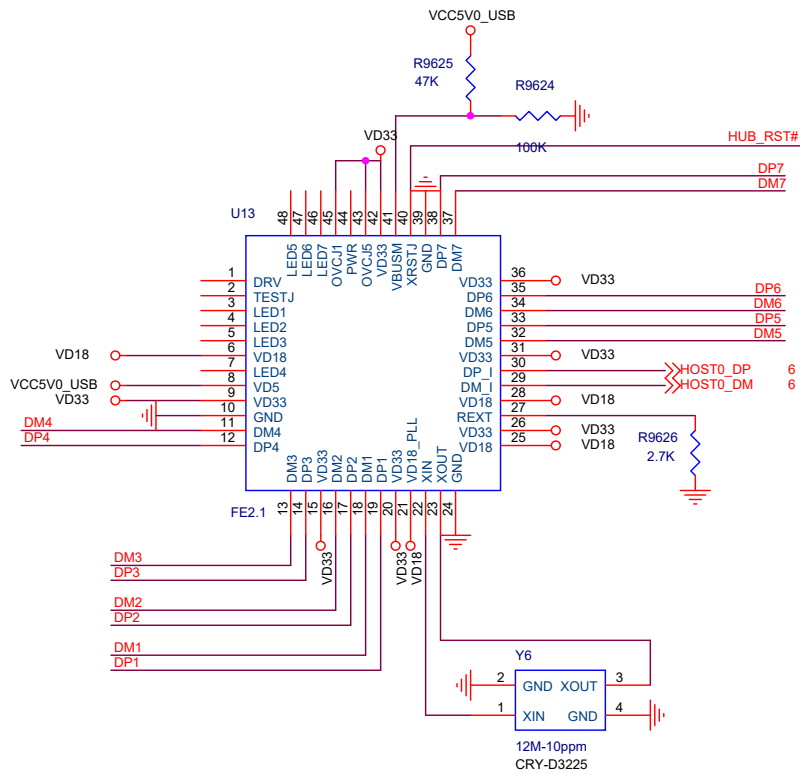


# VCCA\_0V9 Power

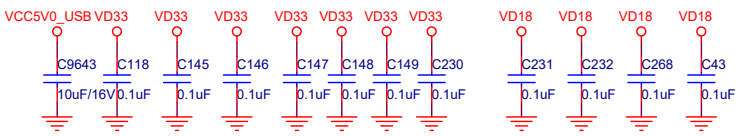
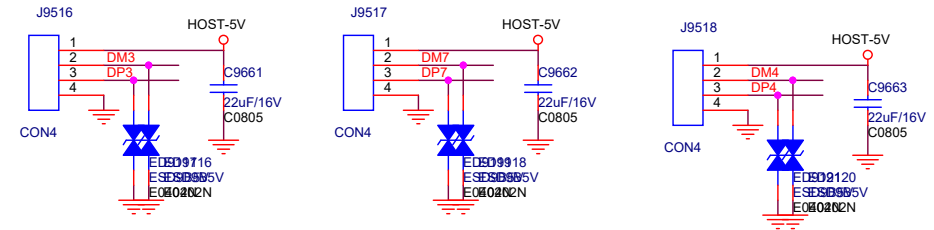


# VCC3V0\_SD Power

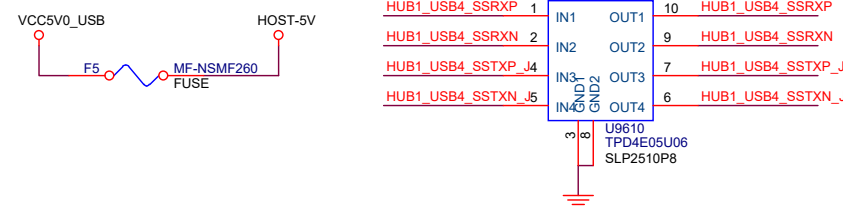
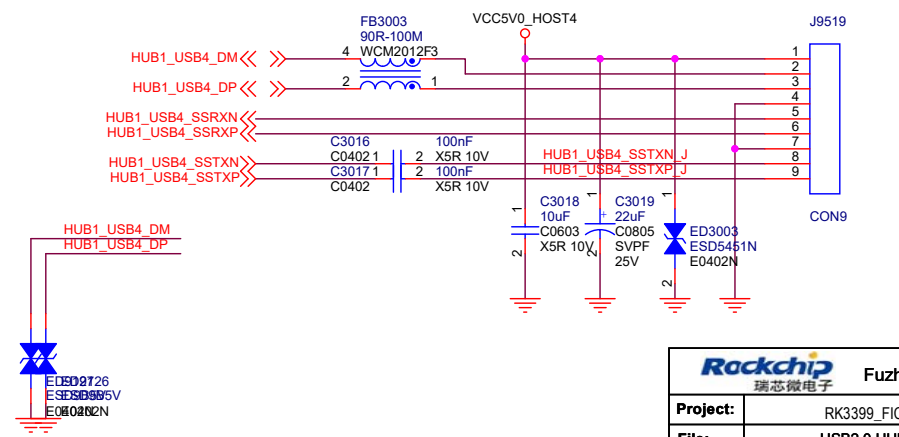




### USB2.0 Port4

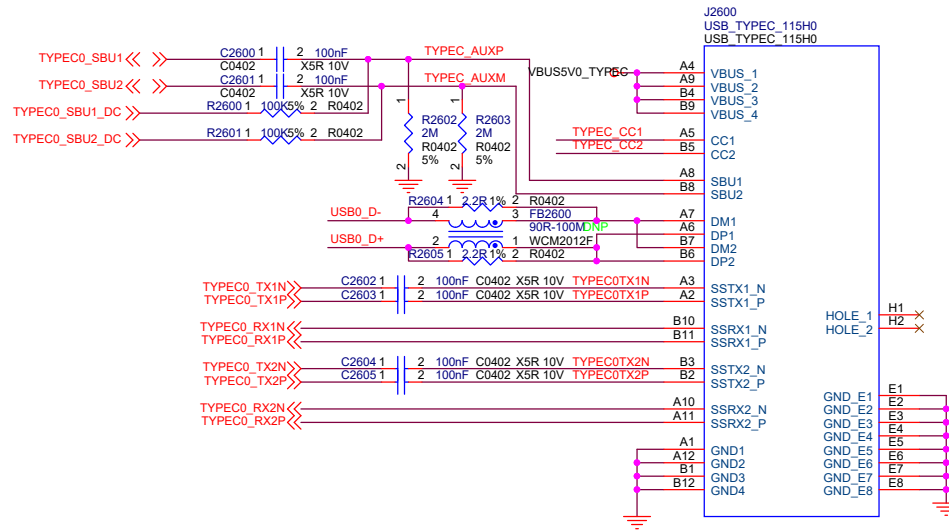


### USB3.0 Port4

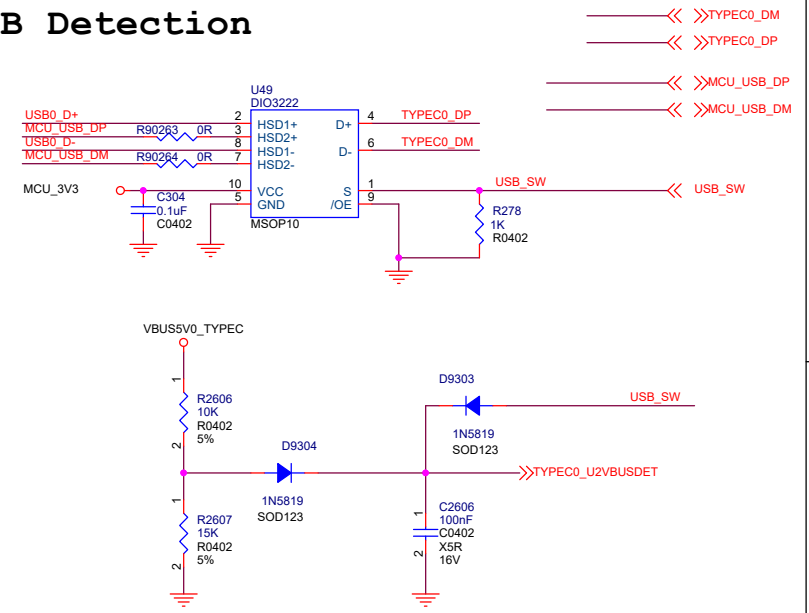


<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	USB2.0 HUB		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	14 of 33

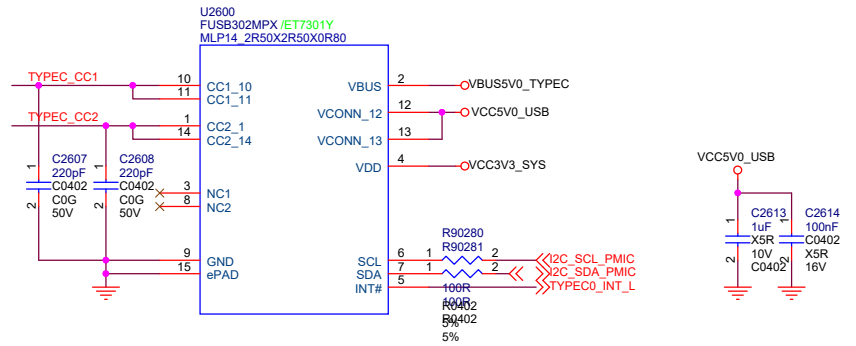
# USB Type-C Port



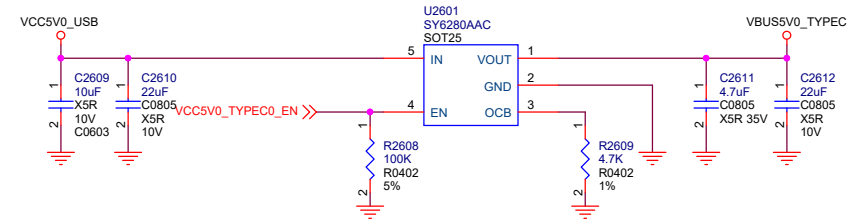
# USB Detection



# USB Type-C CC CTRL

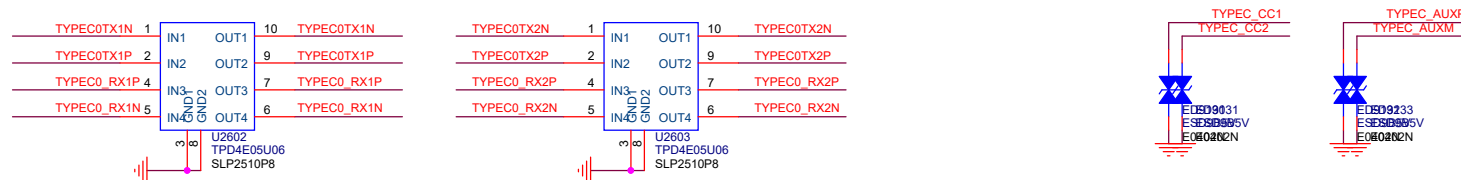


# USB Type-C Power



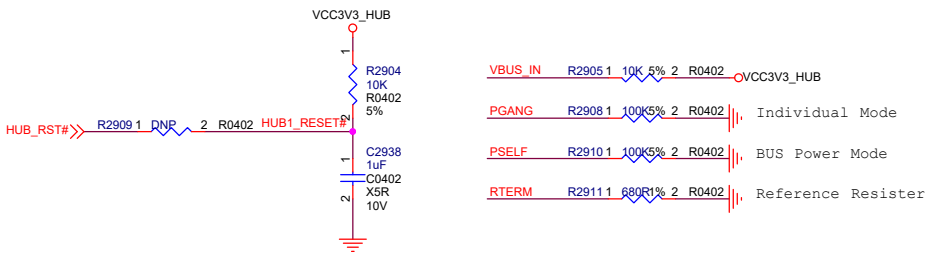
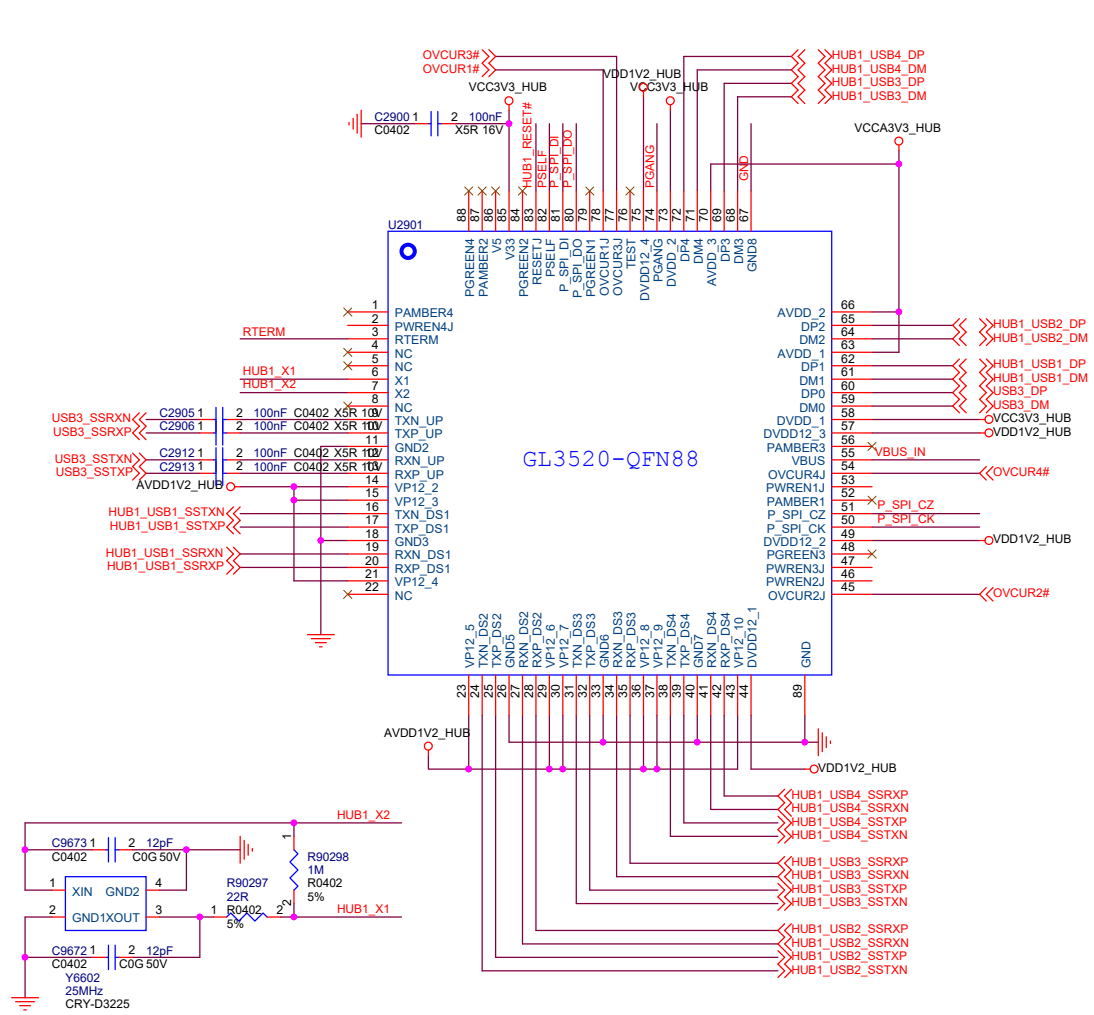
# ESD

Note: All the ESD component should be place close to the port and  $C_j \leq 0.4pF$



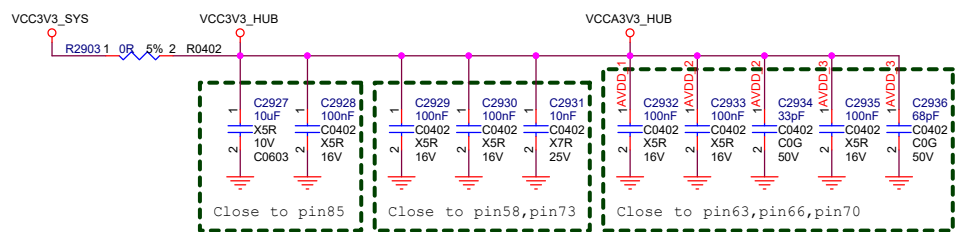
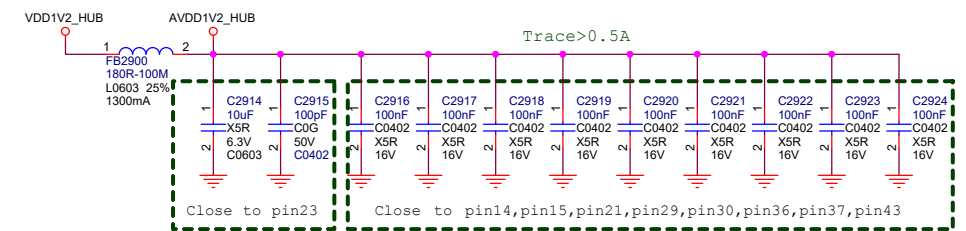
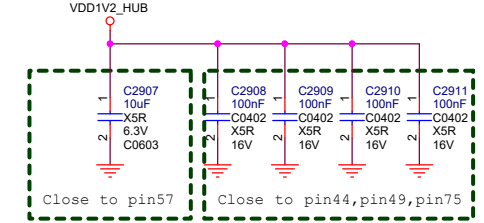
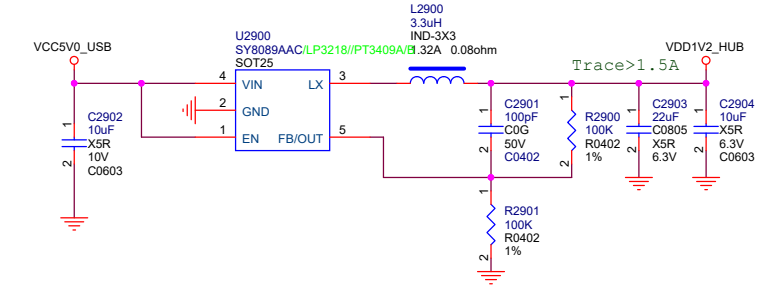
<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	USB Type-C Port		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	15 of 33

# USB3.0 HUB

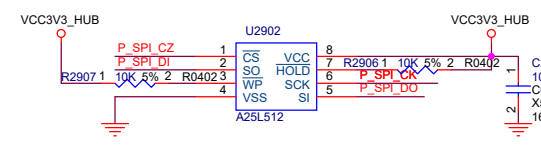


- VBUS\_IN** R2905 1 10K 5% 2 R0402
- PGANG** R2908 1 100K 5% 2 R0402 Individual Mode
- PSELF** R2910 1 100K 5% 2 R0402 BUS Power Mode
- RTERM** R2911 1 80R 1% 2 R0402 Reference Resistor

# HUB Power



# SPI Flash

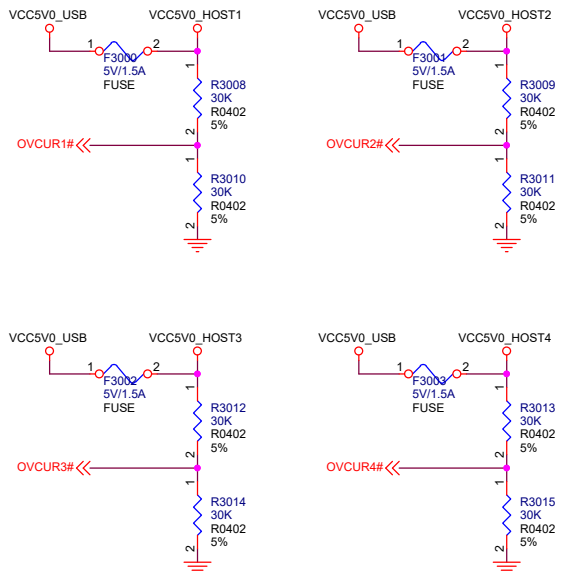


<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	USB3.0 HUB-GL3523-1 (option)		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	16 of 33



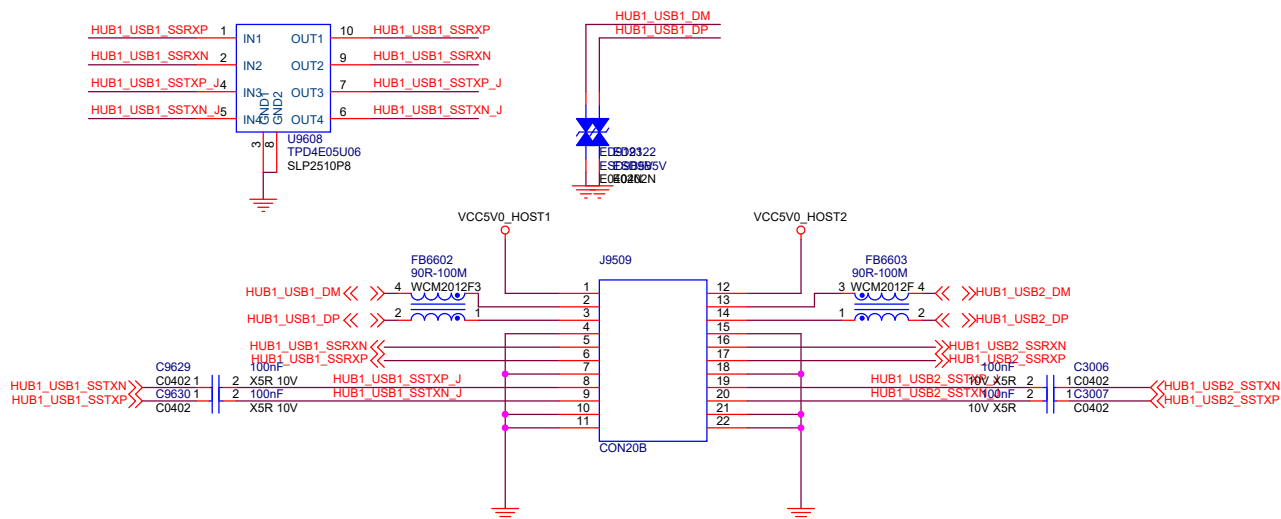
## Option2

POLY-FUSE CIRCUIT

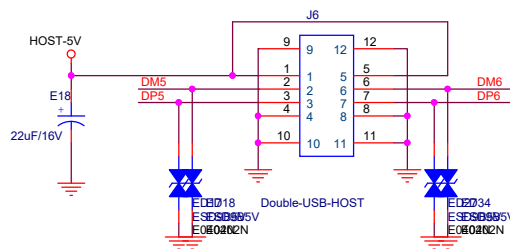
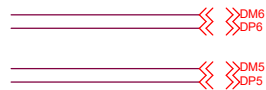
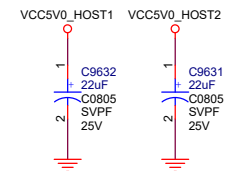
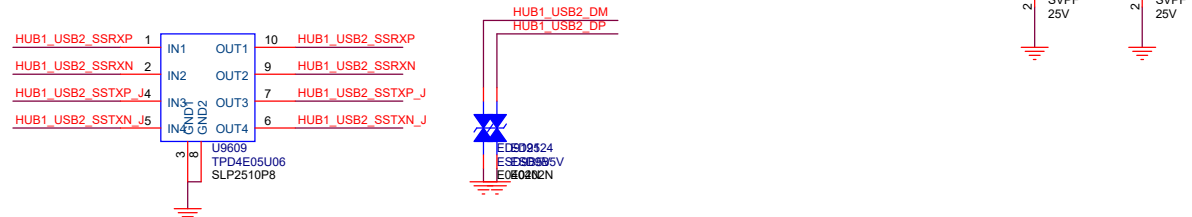


OVCUR1#~4# Floating : Non-Removable (Compound device)

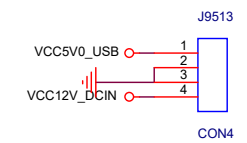
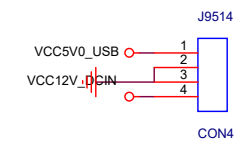
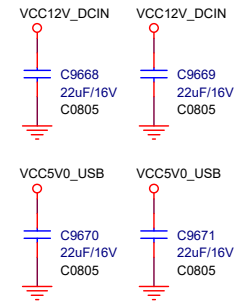
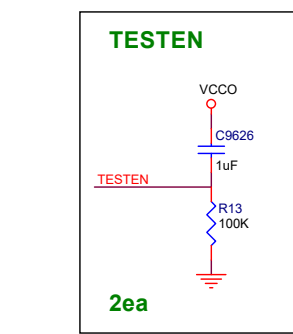
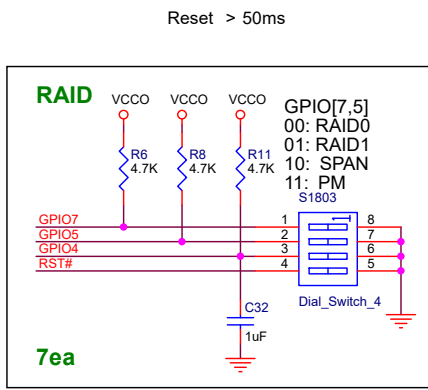
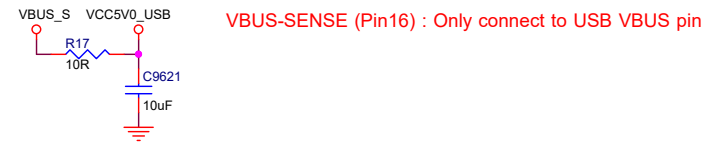
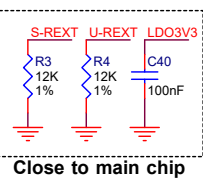
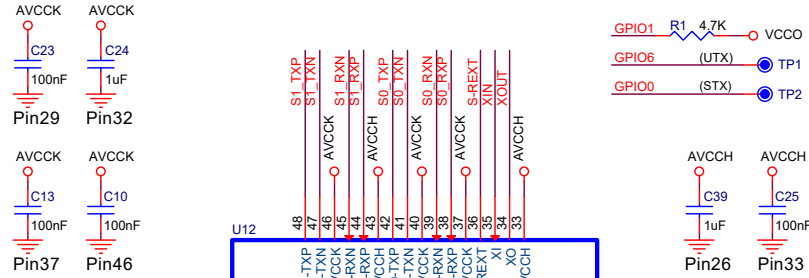
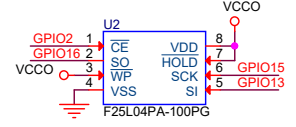
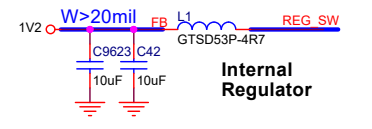
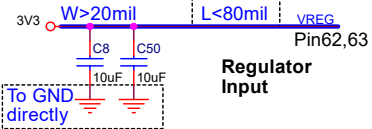
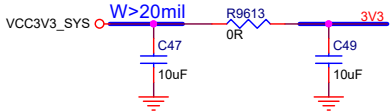
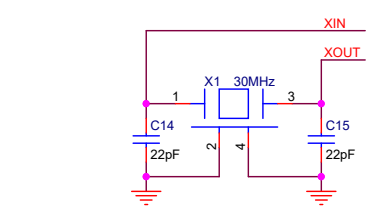
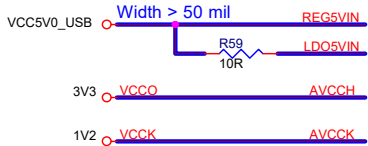
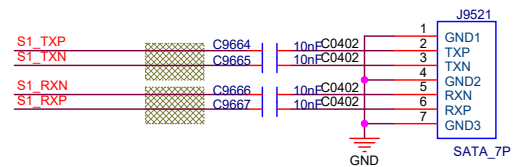
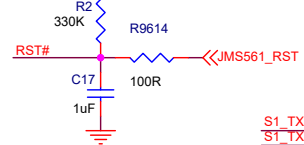
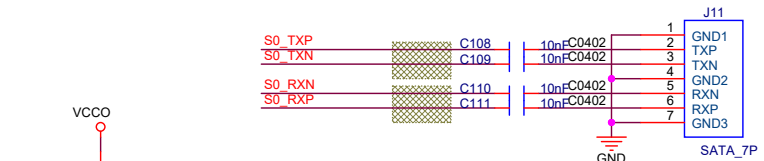
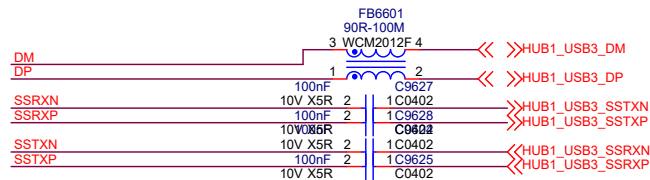
## USB3.0 Port1



## USB3.0 Port2

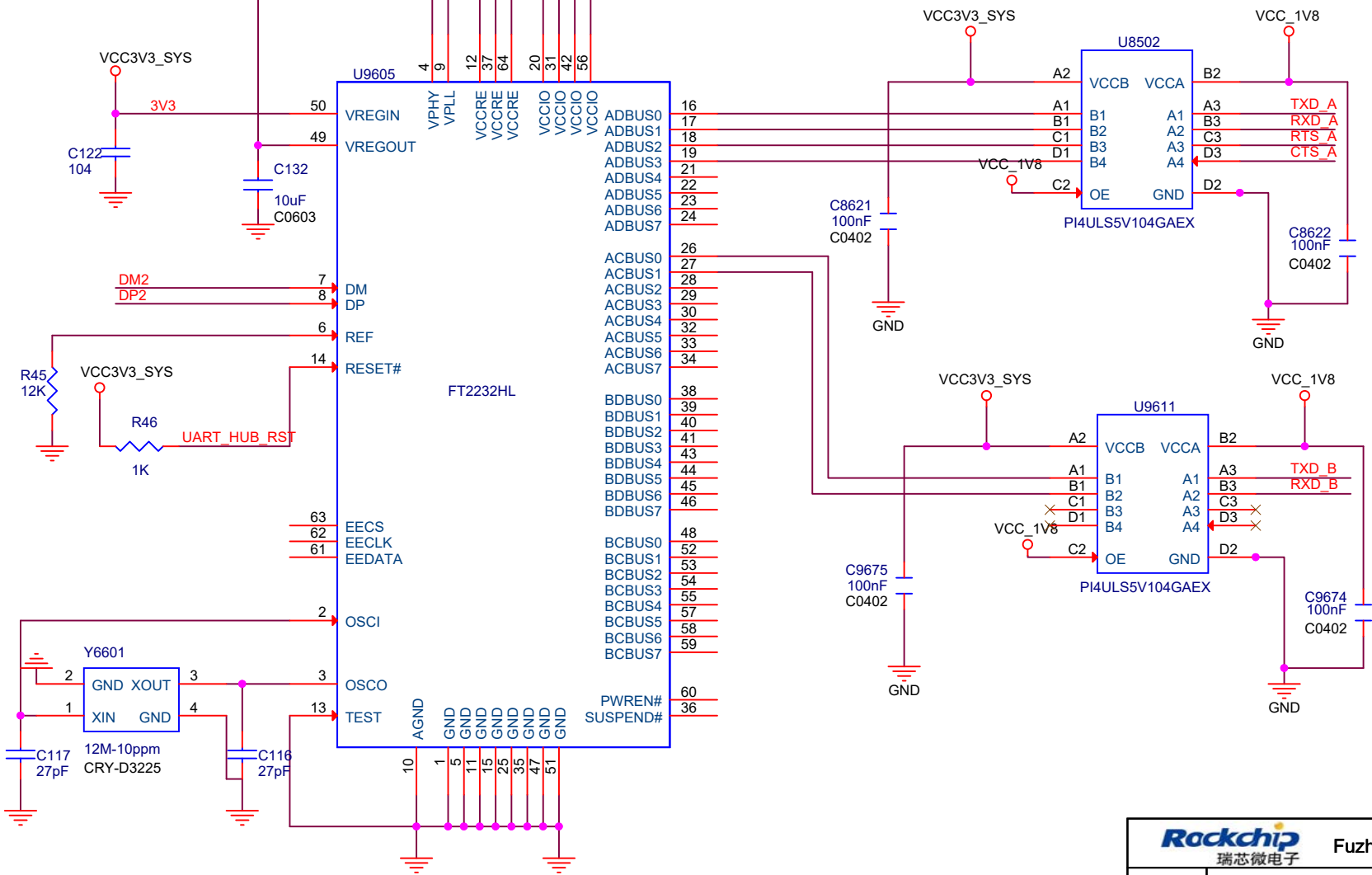
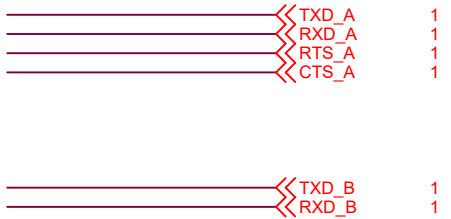
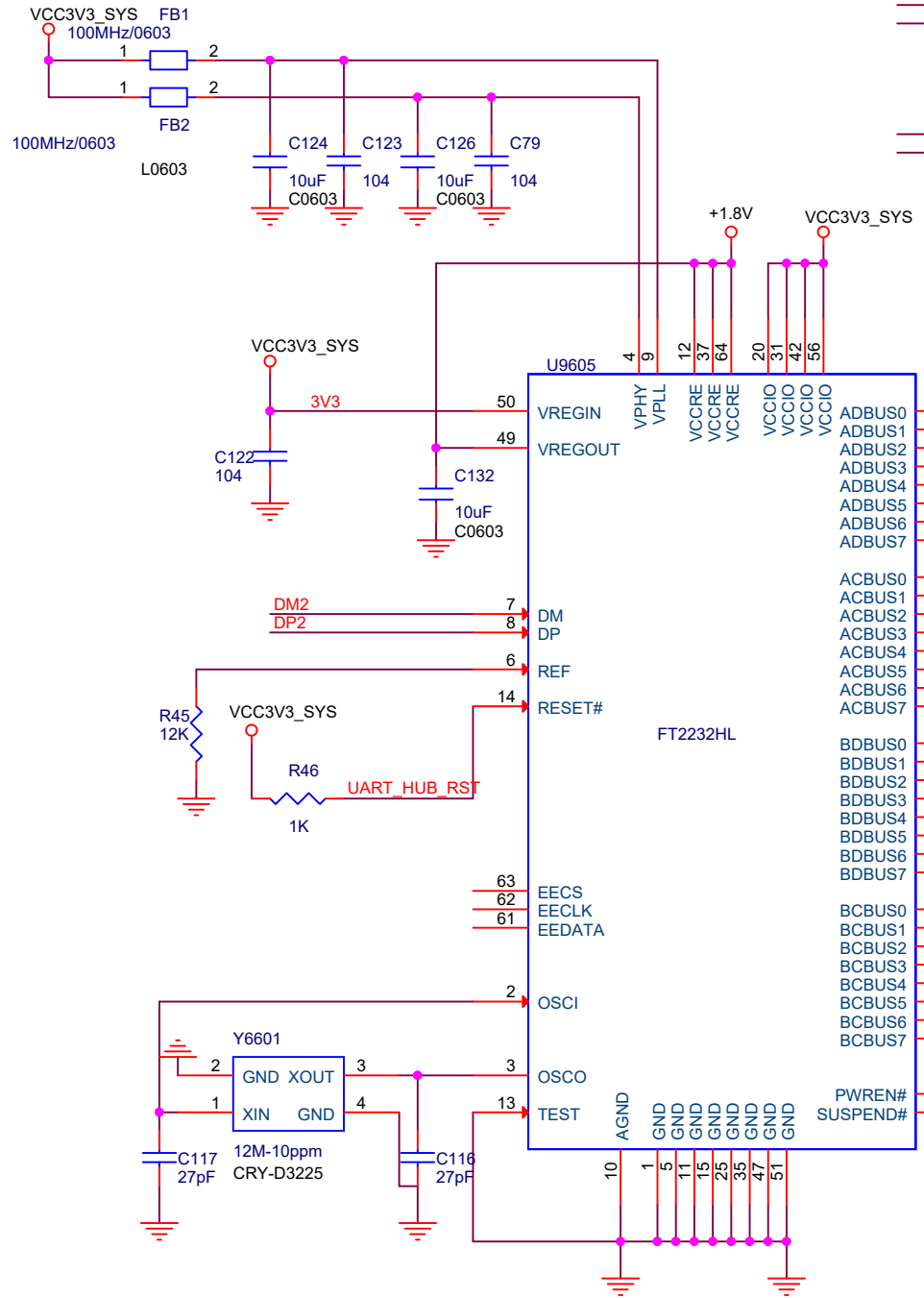



<b>Rockchip</b> 瑞芯微电子		Fuzhou Rockchip Electronics	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	USB3.0 HUB-GL3523-2 (option)		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	17 of 33



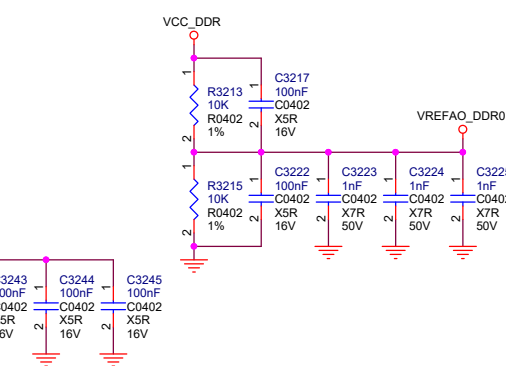
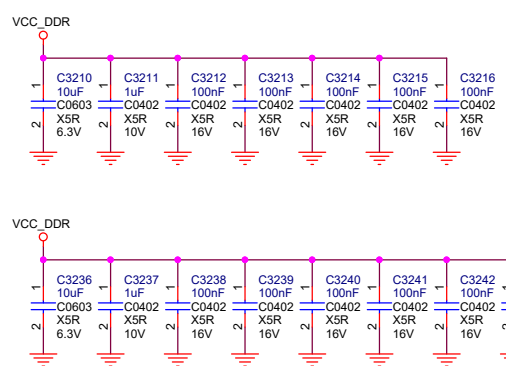
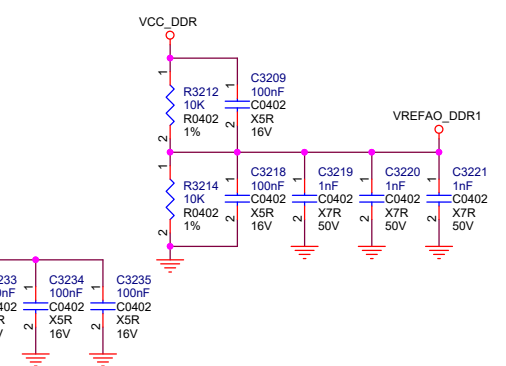
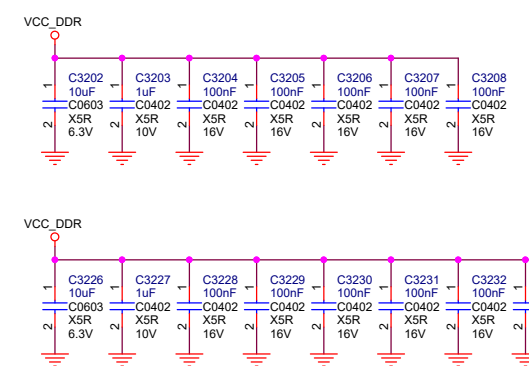
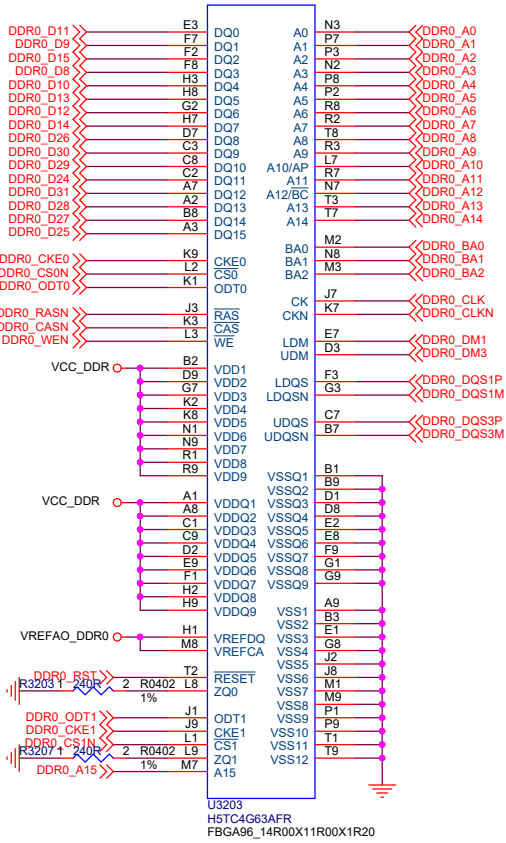
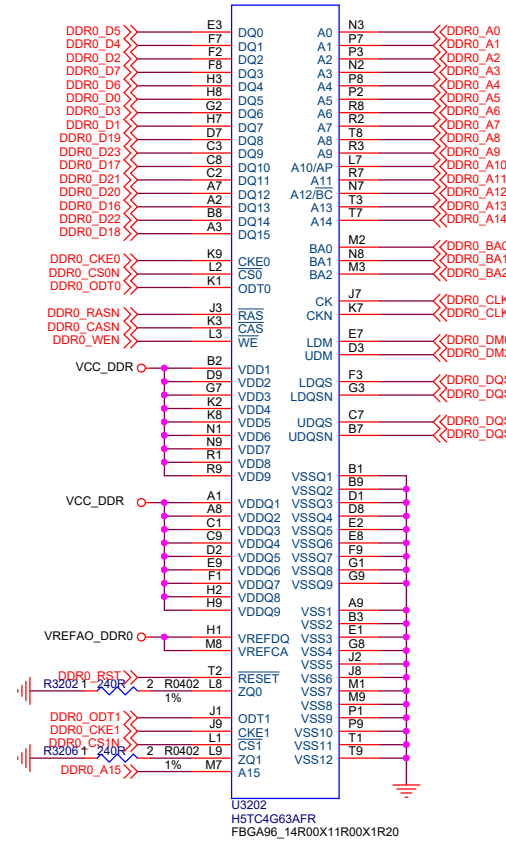
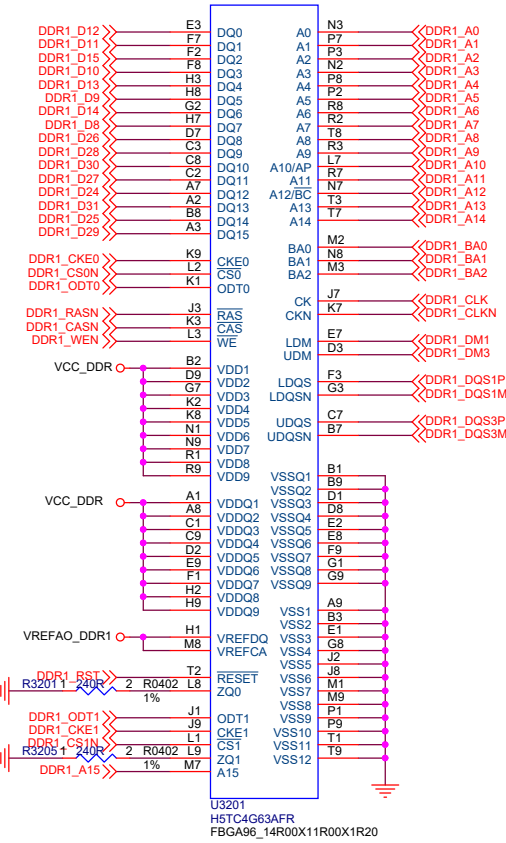
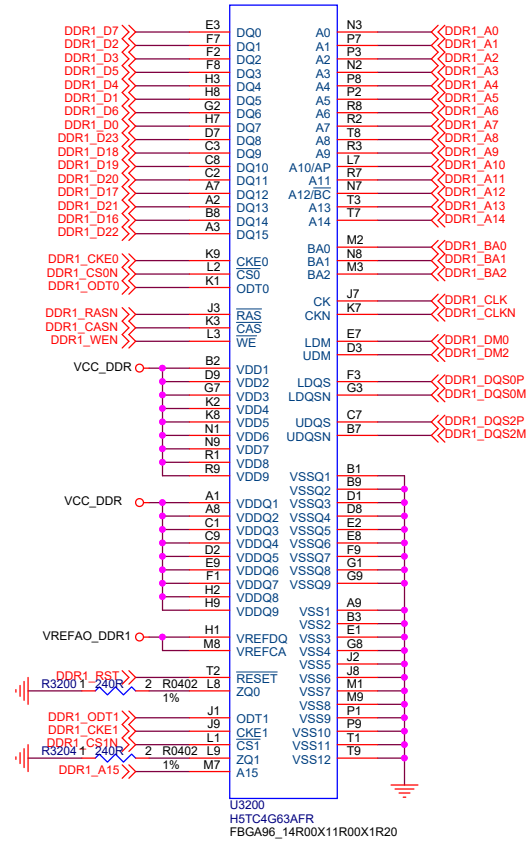
VBUS-SENSE (Pin16) : Only connect to USB VBUS pin

<b>Rackchip</b> 瑞芯微电子 Fuzhou Rockchip Electronics	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	USB TO SATA
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	18 of 33



 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	USB TO UART
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	19 of 33

# DDR3 4x16bit

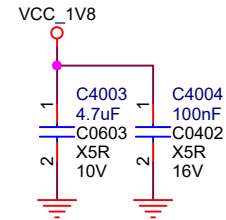
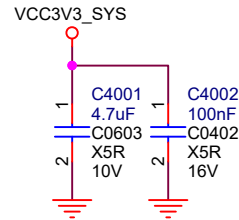
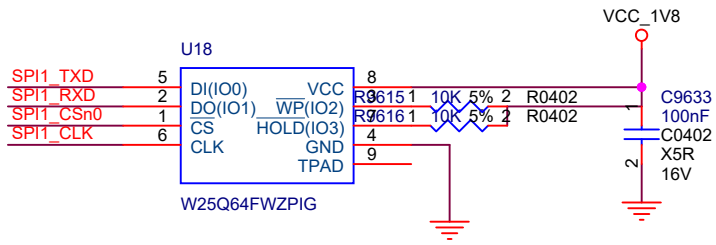
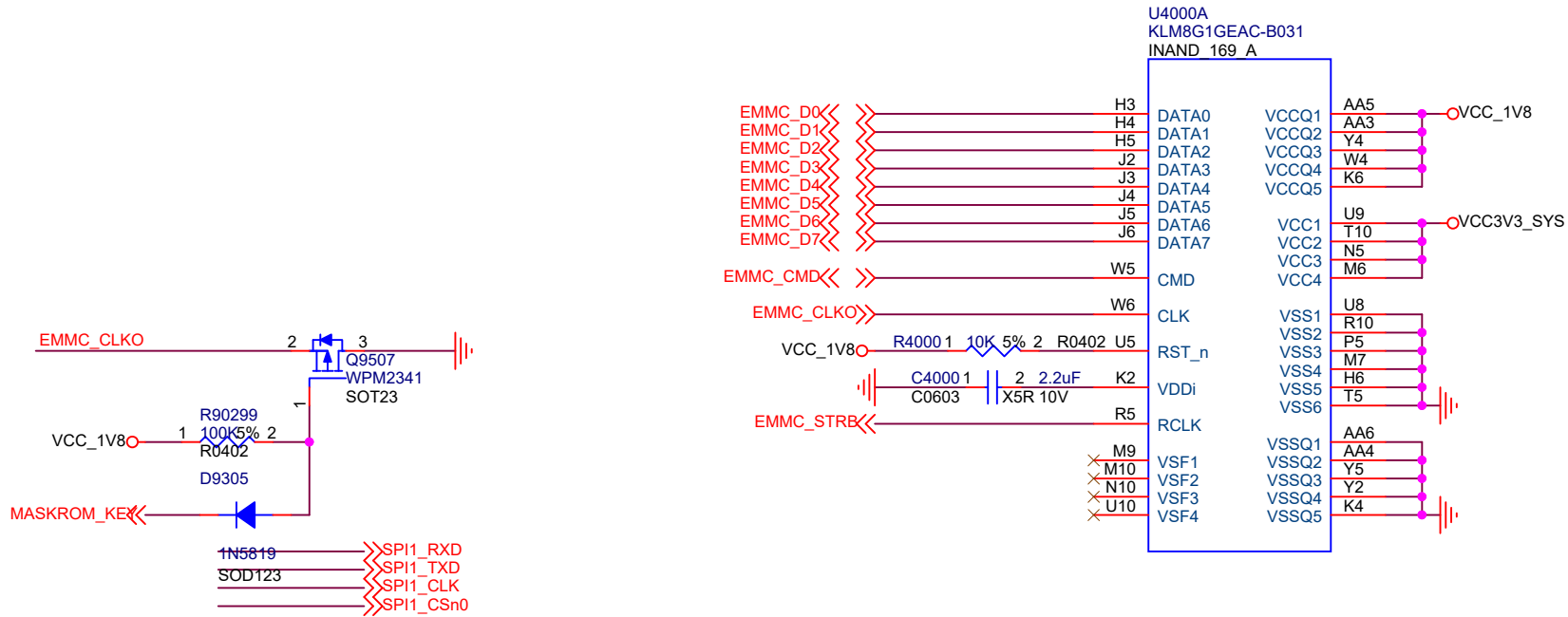


Note: All the Power filter capacitor should be place close to the power pin of DDR

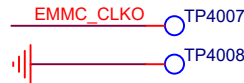
Note: All the Power filter capacitor should be place close to the power pin of DDR


<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	RAM-DDR3 4x16bit(option)		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	20 of 33

# eMMC FLASH



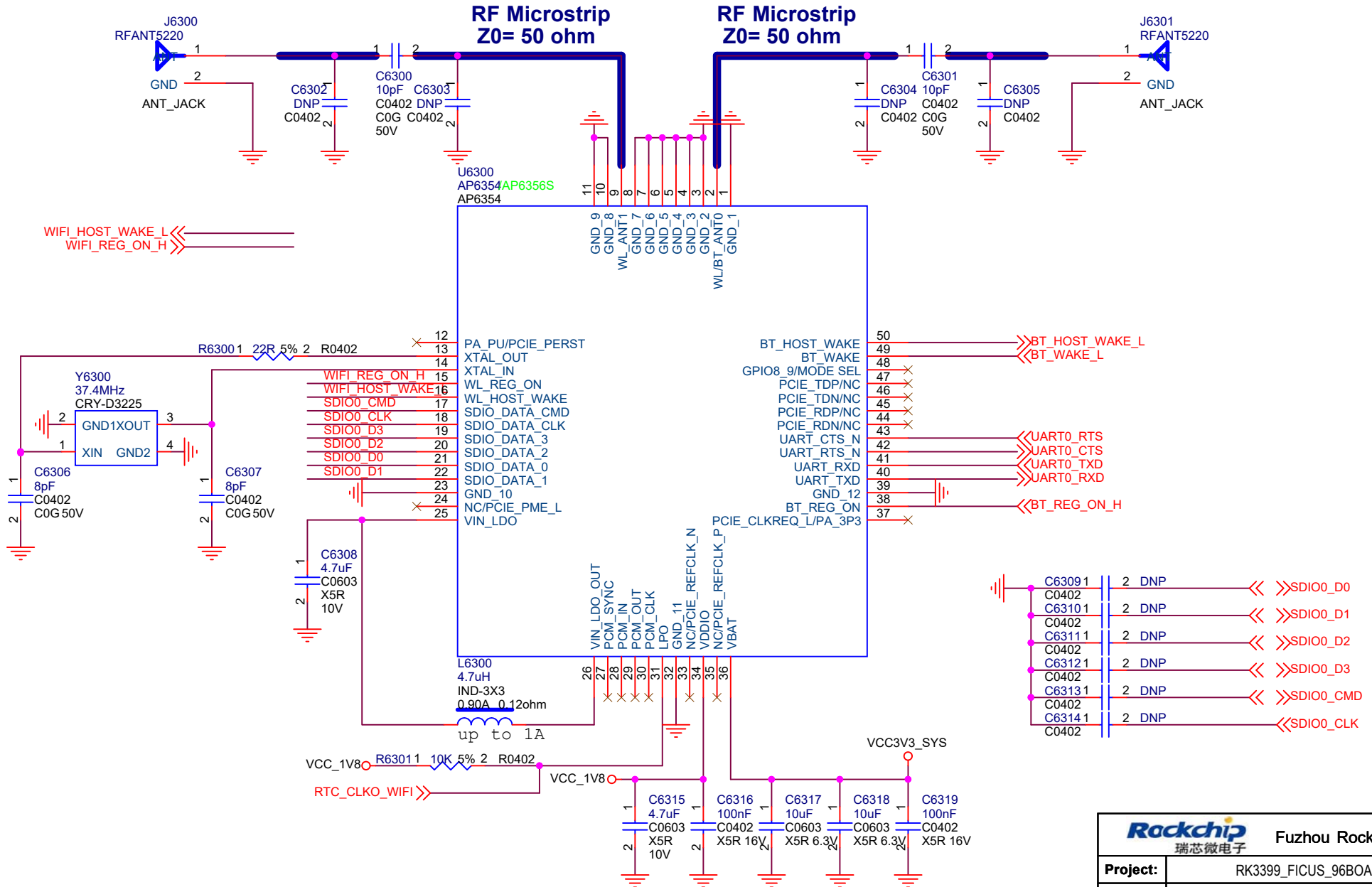
Note:  
Reserve PAD for Update.




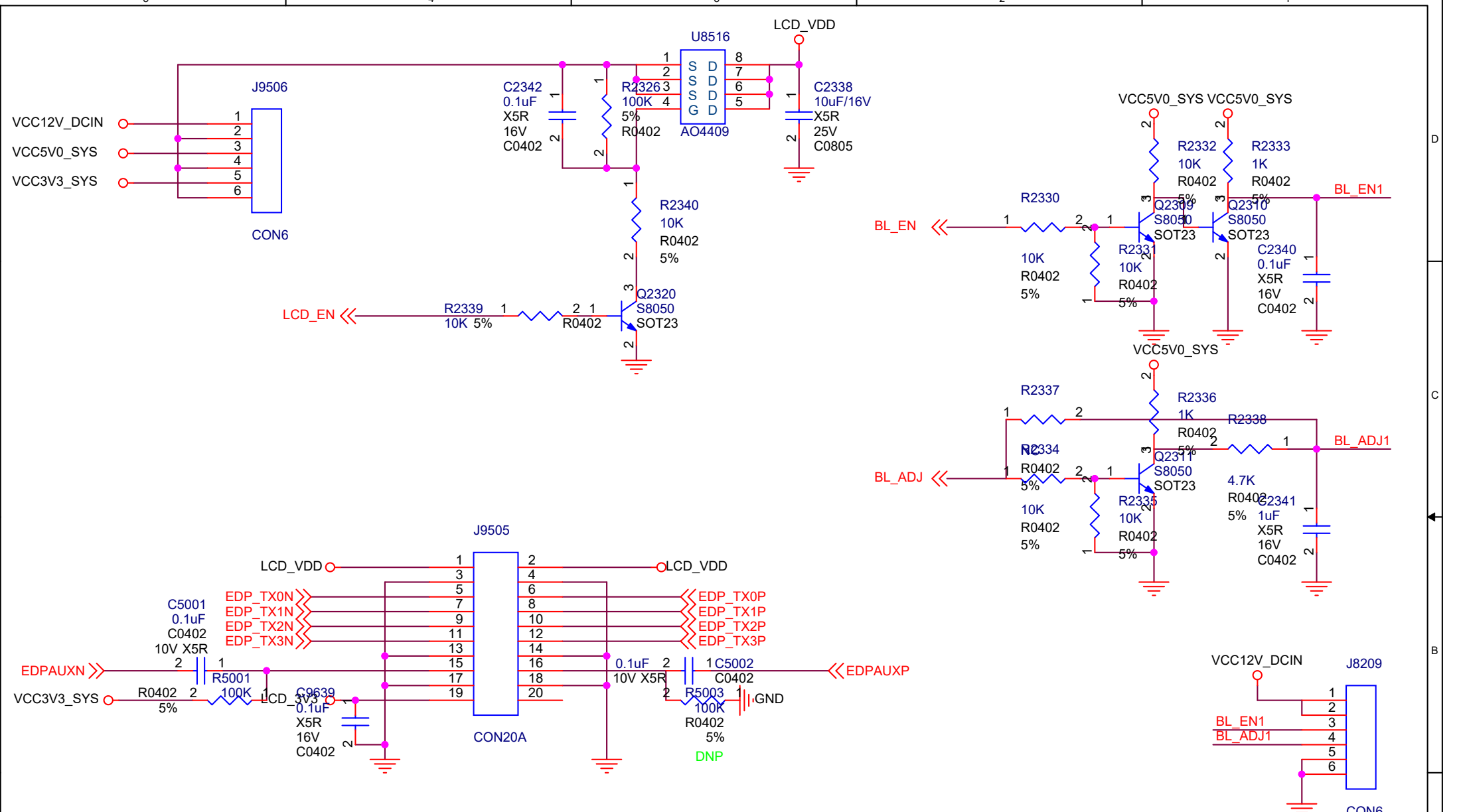
 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	Memory-eMMC
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	21 of 33


# SDIO WIFI/BT MODULE-MIMO

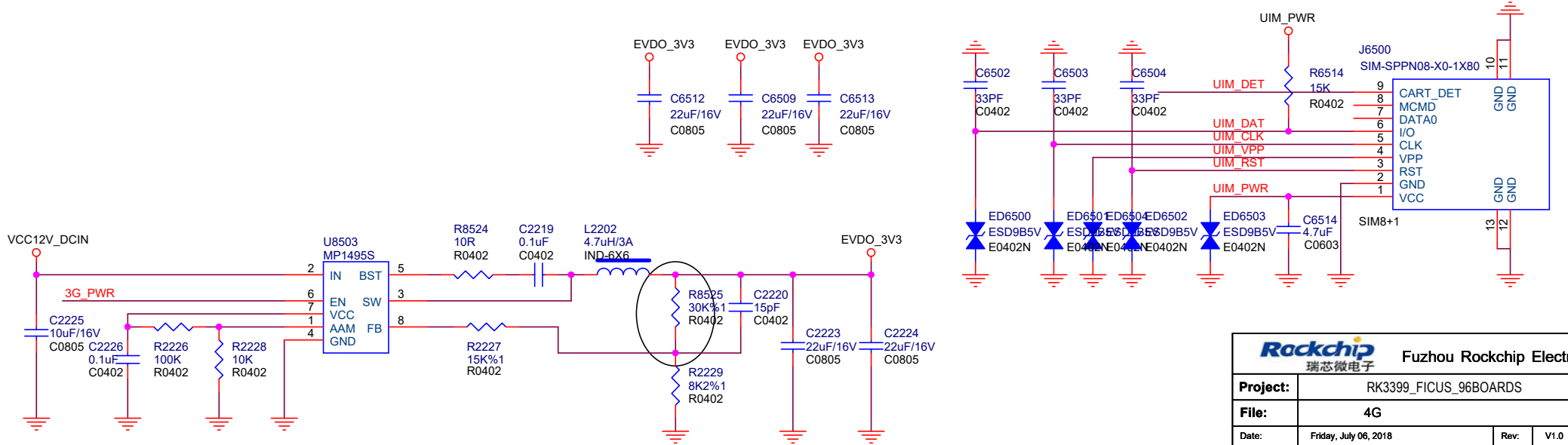
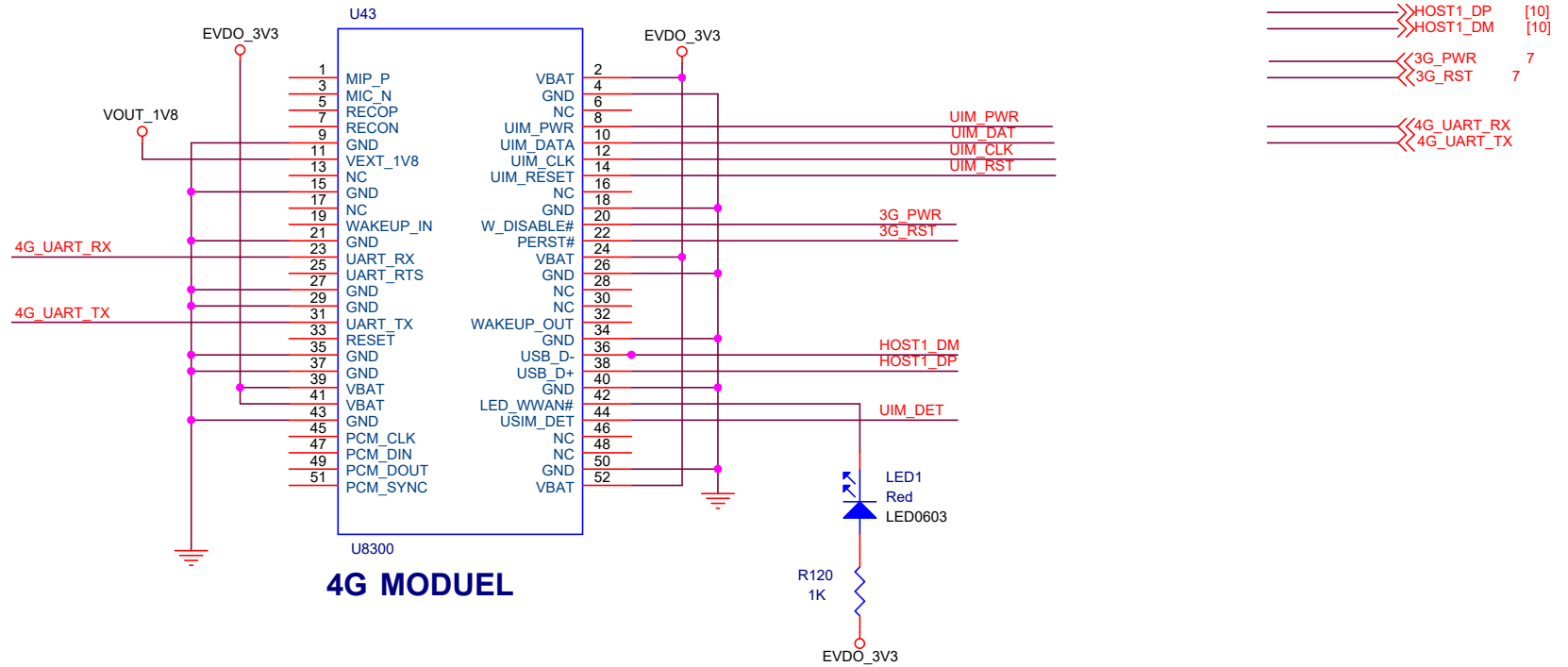
Note: VBAT voltage range is 3.0V~4.8V,  
and peak current is at least 400mA.



 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	WIFI/BT MIMO-AP63xx
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
<b>Rev:</b>	V1.0
<b>Sheet:</b>	22 of 33



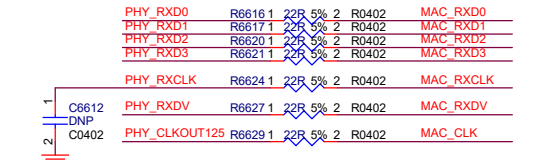
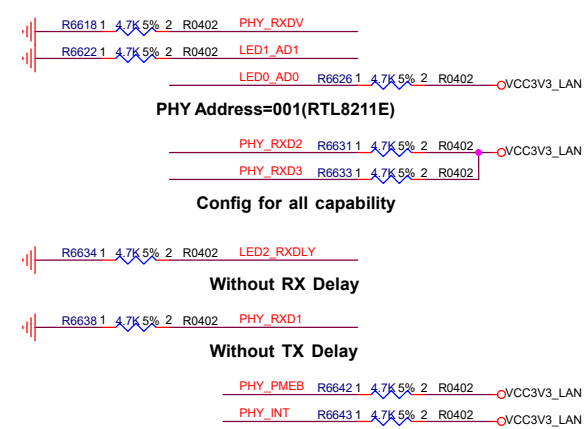
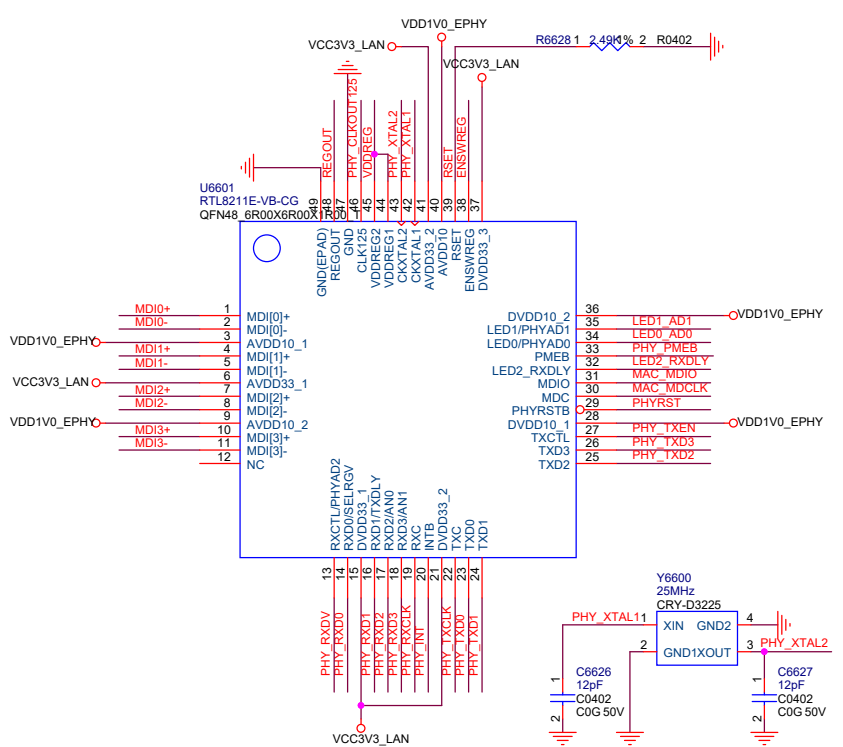
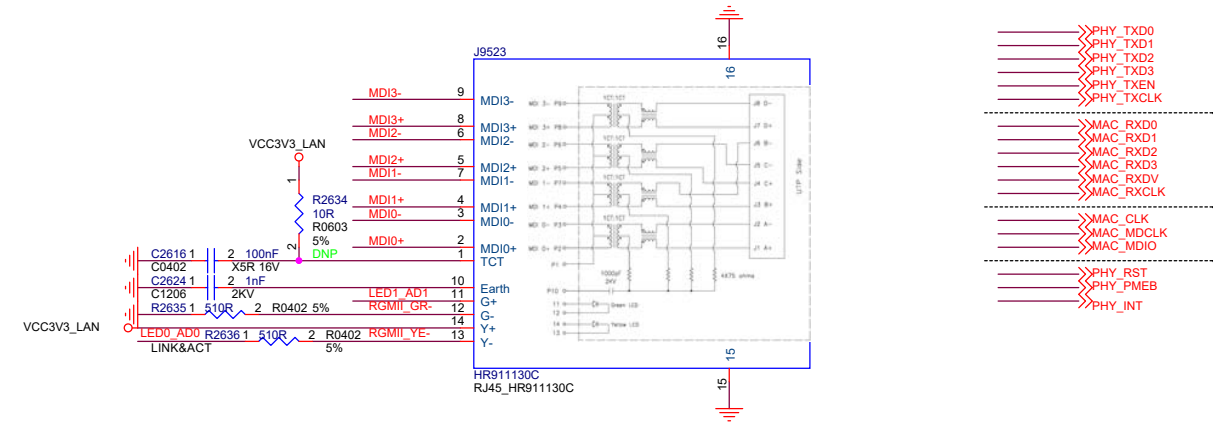
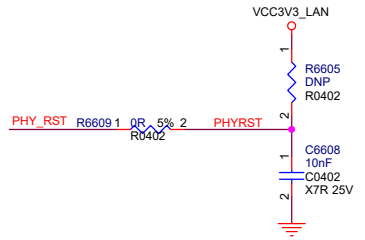
 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	EDP
<b>Date:</b>	Friday, July 06, 2018
<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus
<b>Sheet:</b>	23 of 33



<b>Rackchip</b> 瑞芯微电子 Fuzhou Rockchip Electronics			
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	4G		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	24 of 33



# GMAC 10/100/1000 RGMII Ethernet PHY



**Close to PHY**

PHY\_RXD0 R6616 1 22R 5% 2 R0402 MAC\_RXD0  
 PHY\_RXD1 R6617 1 22R 5% 2 R0402 MAC\_RXD1  
 PHY\_RXD2 R6620 1 22R 5% 2 R0402 MAC\_RXD2  
 PHY\_RXD3 R6621 1 22R 5% 2 R0402 MAC\_RXD3

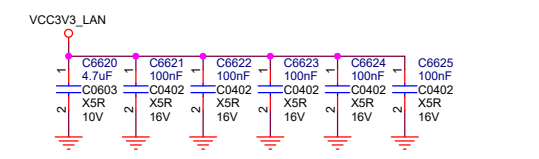
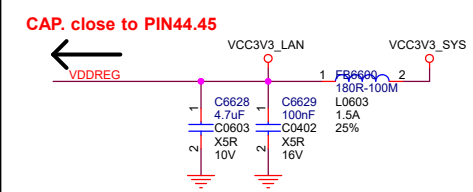
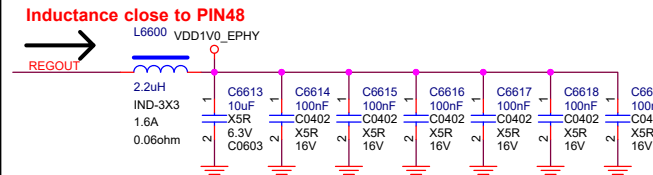
PHY\_RXCLK R6624 1 22R 5% 2 R0402 MAC\_RXCLK  
 PHY\_RXDV R6627 1 22R 5% 2 R0402 MAC\_RXDV  
 PHY\_CLKOUT125 R6629 1 22R 5% 2 R0402 MAC\_CLK

PHY\_RXD0 R6637 1 4.7K 5% 2 R0402 VCC3V3\_LAN

ENSWREG R6641 1 0R 5% 2 R0402 VCC3V3\_LAN

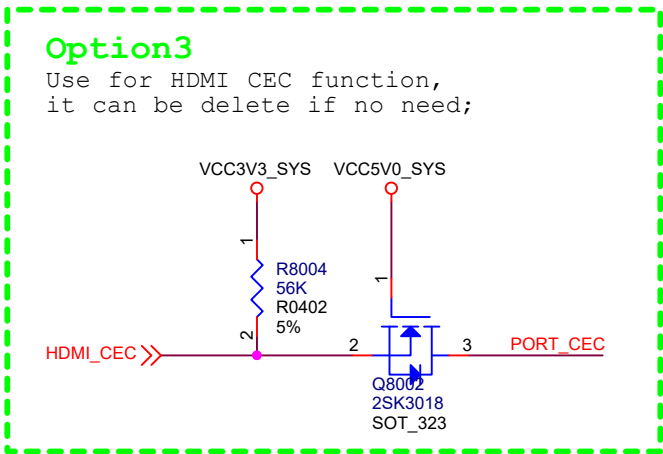
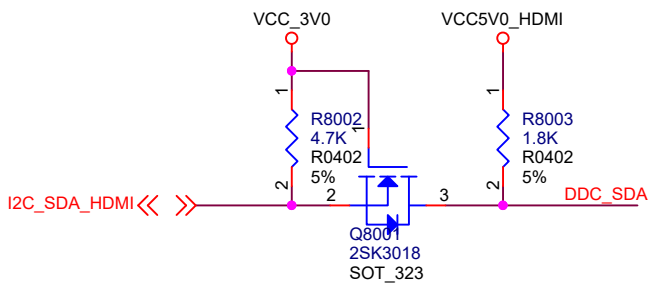
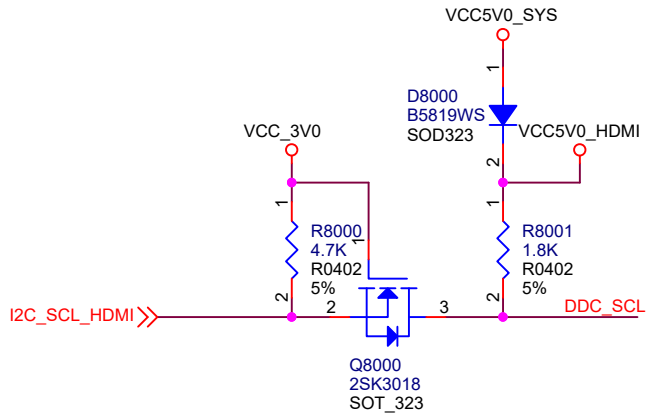
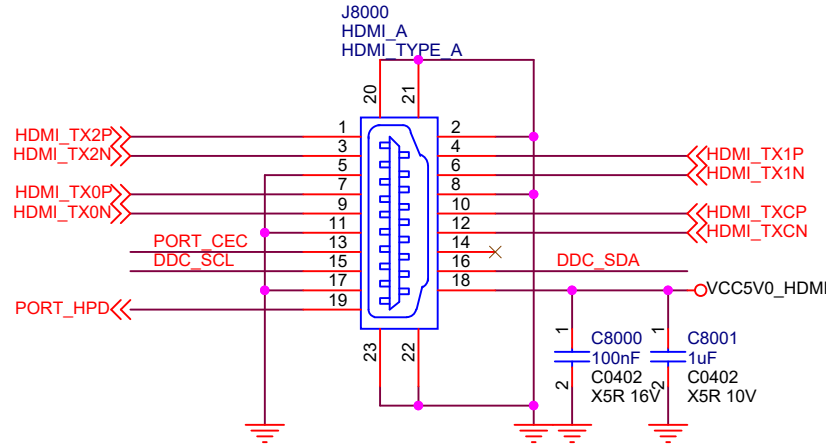
**Pull down for 2.5V RGMII (RTL8211D/8211E)  
 Pull up for 3.3V RGMII (RTL8211D/8211E)  
 Pull up 1.5 / 1.8V RGMII (RTL8211E-VL only)**

Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.



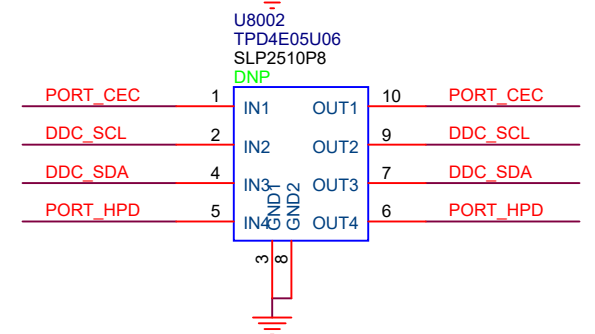
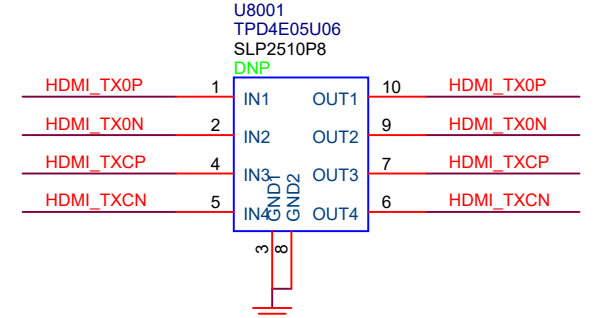
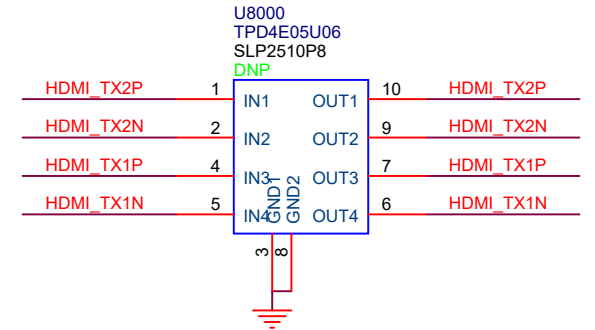
<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	GMAC-RTL8211E		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	25 of 33

# HDMI Output



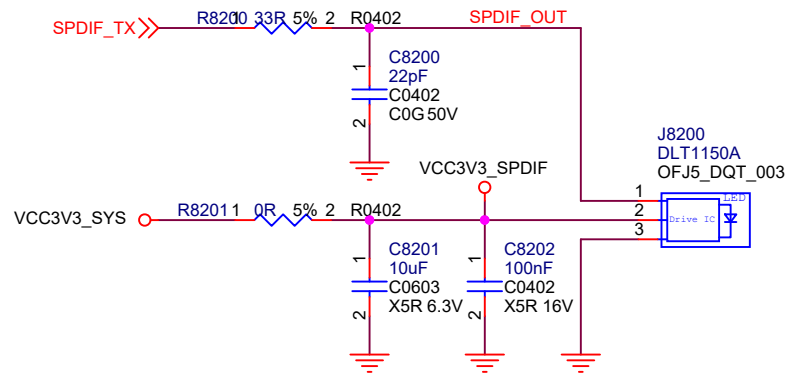
# ESD


Note: All the ESD component should place close to the port and  $C_j \leq 0.4\text{pF}$



<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	HDMI Output		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
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# SPDIF OUT



 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子			
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	SPDIF Output		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	27 of 33

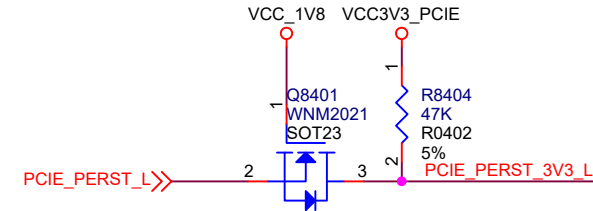
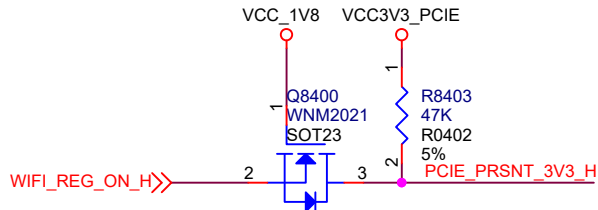
# PCIe Slot-x4

Note: VCC3V3\_PCIE peak current is at least 1.5A.

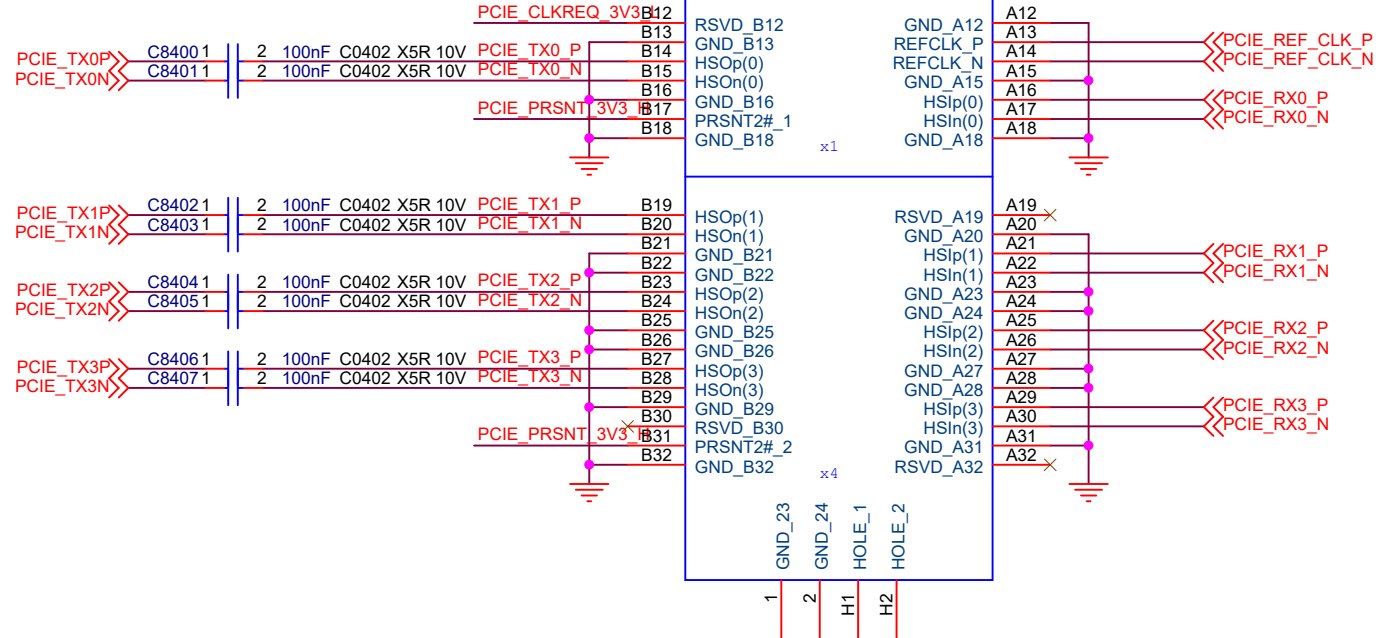
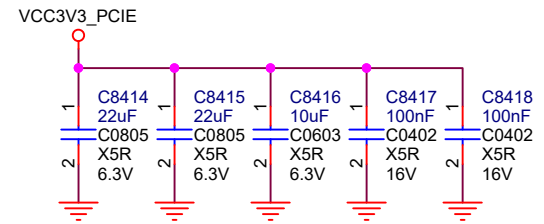
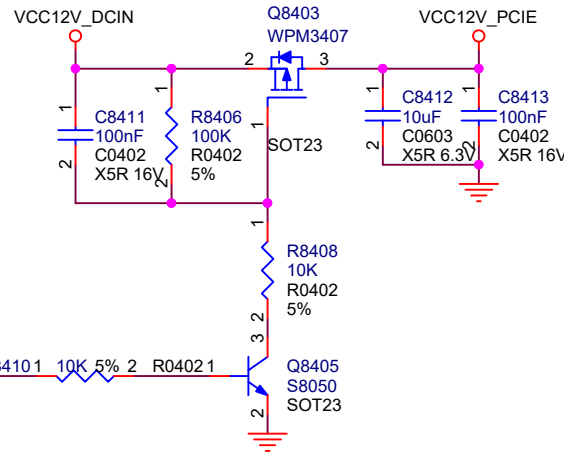
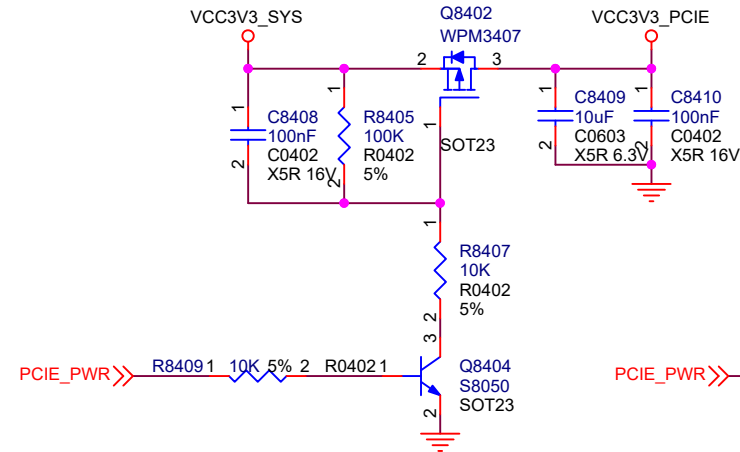
PCIE\_CLKREQ\_L << R84011 22R 5% 2 R0402 PCIE\_CLKREQ\_3V3\_L

WIFI\_HOST\_WAKE\_L << R84021 22R 5% 2 R0402 PCIE\_WAKE\_3V3\_L

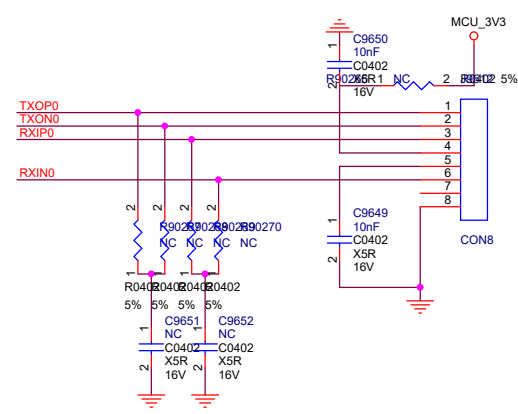
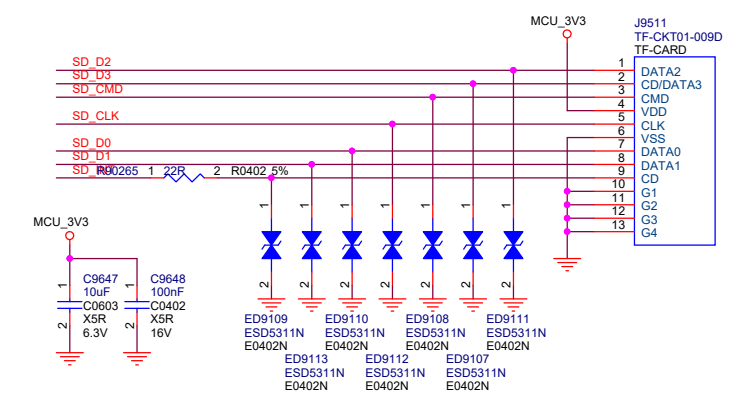
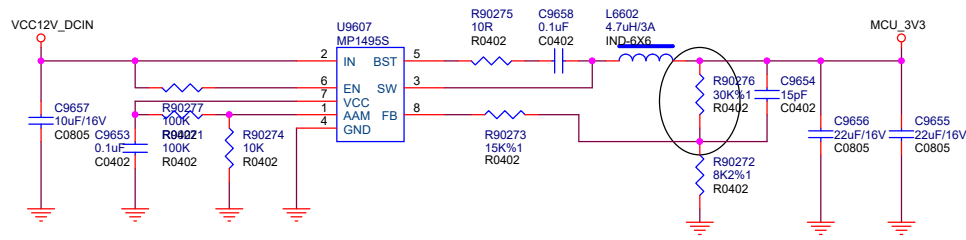
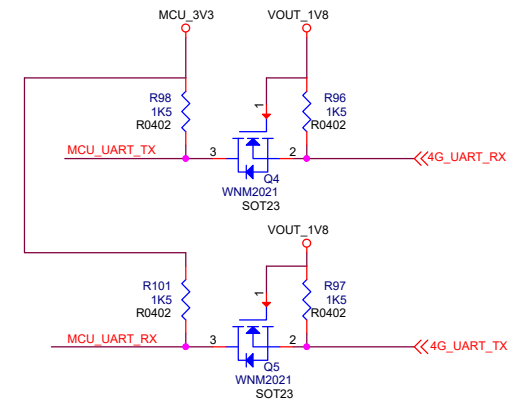
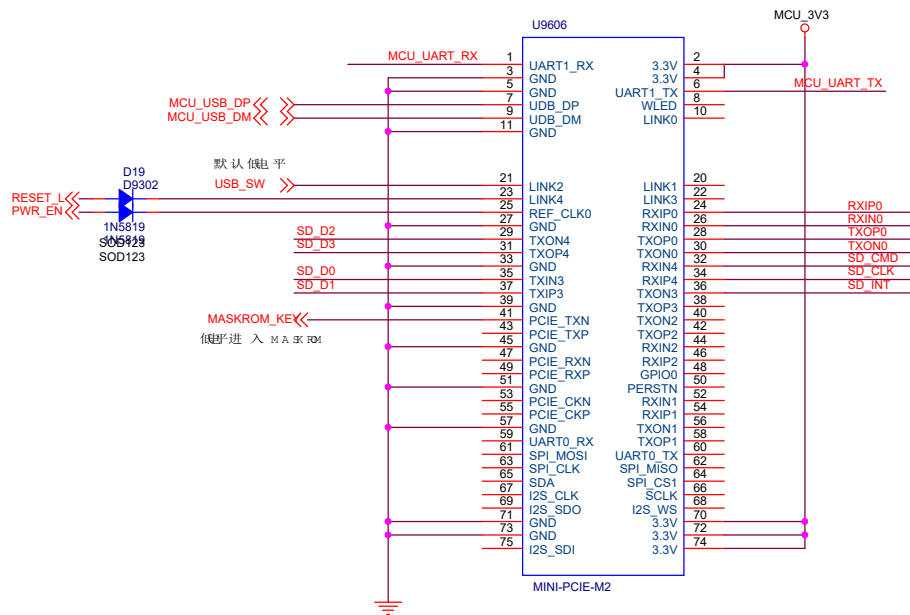
From WIFI OD output to RK3399



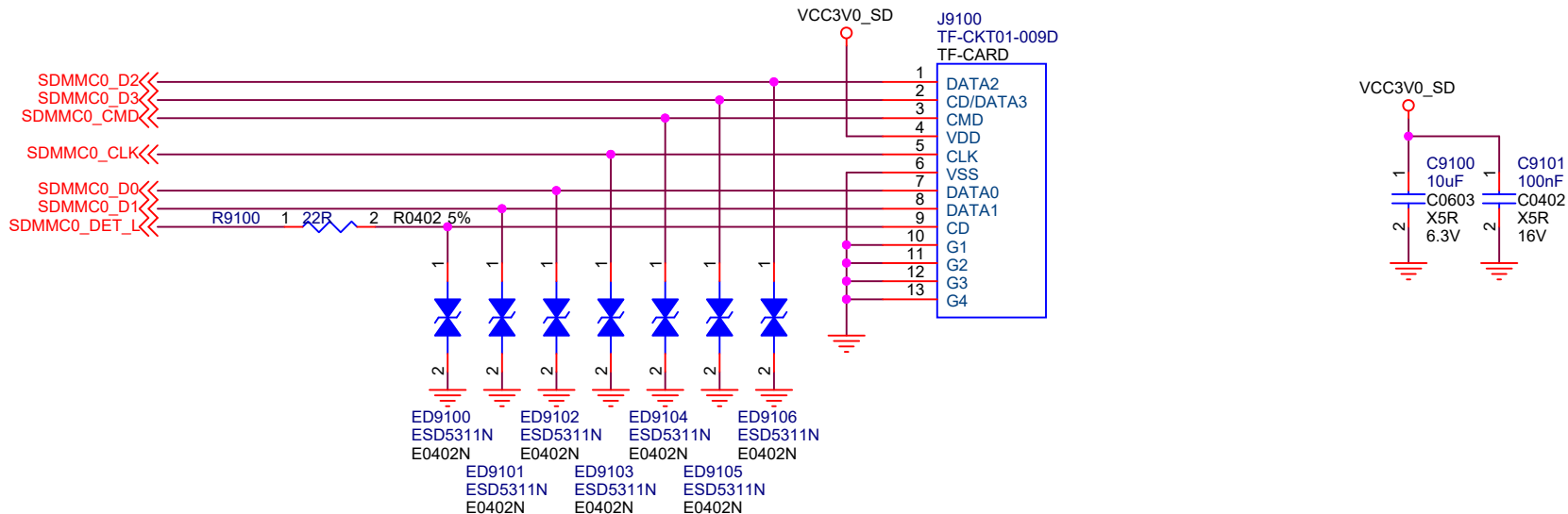
From RK3399 output to WIFI



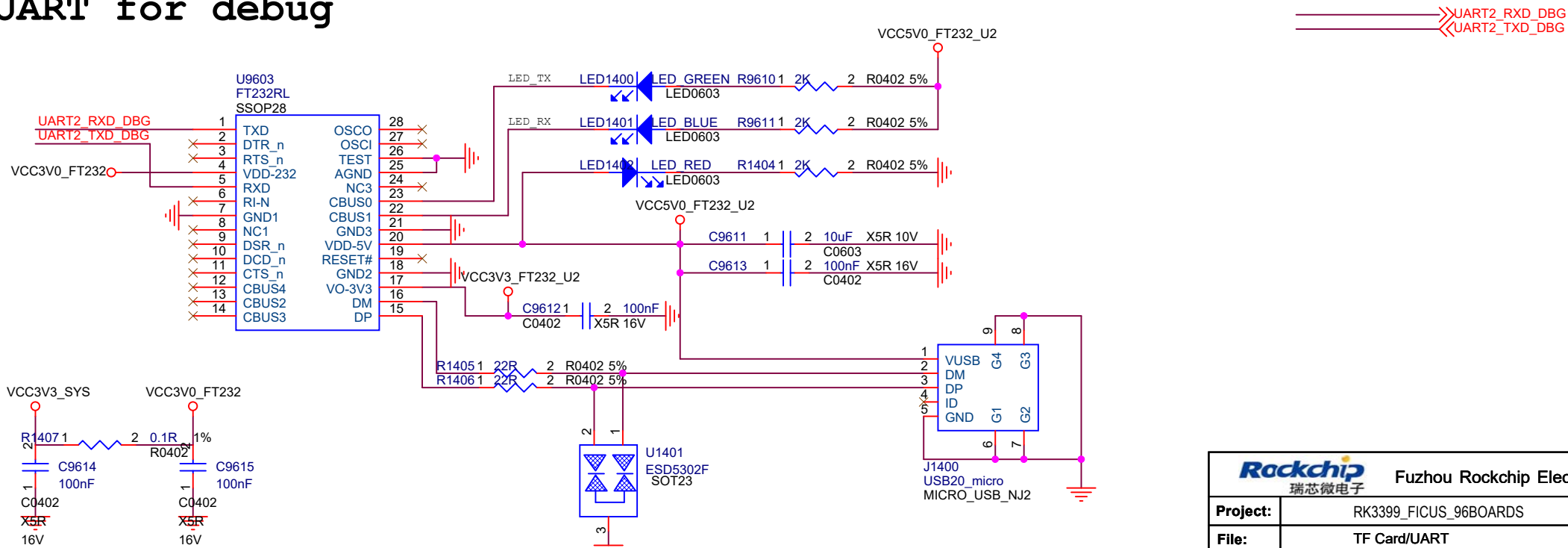
<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	PCIe Slot-x16 (option)		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
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# TF CARD

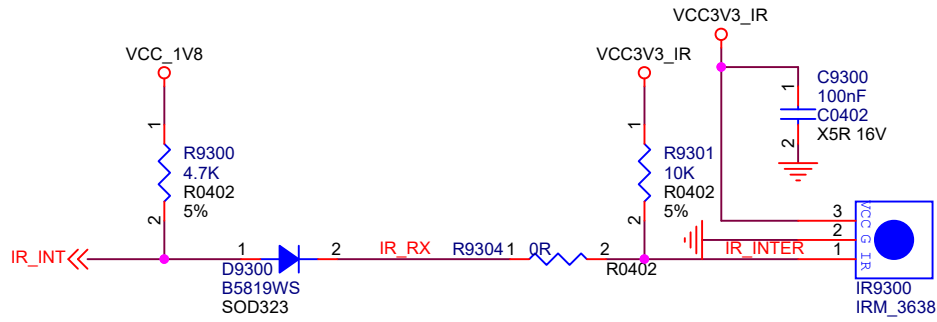


# UART for debug

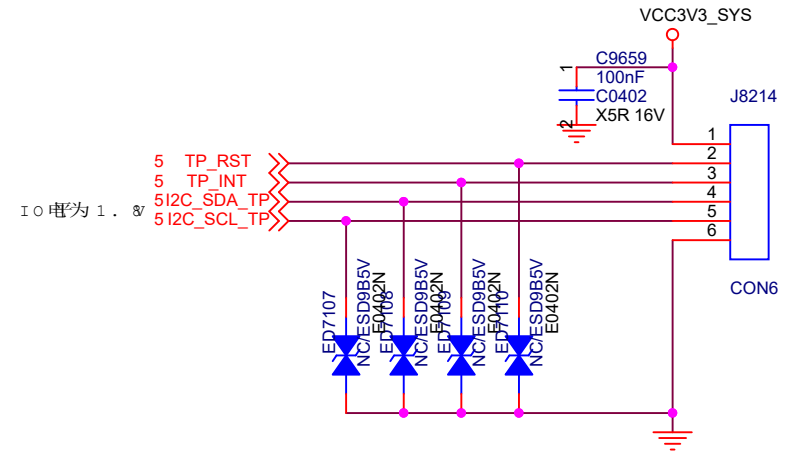


 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	TF Card/UART
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
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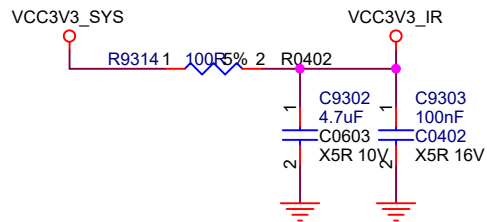
# IR Receiver




# TP



# IR Power

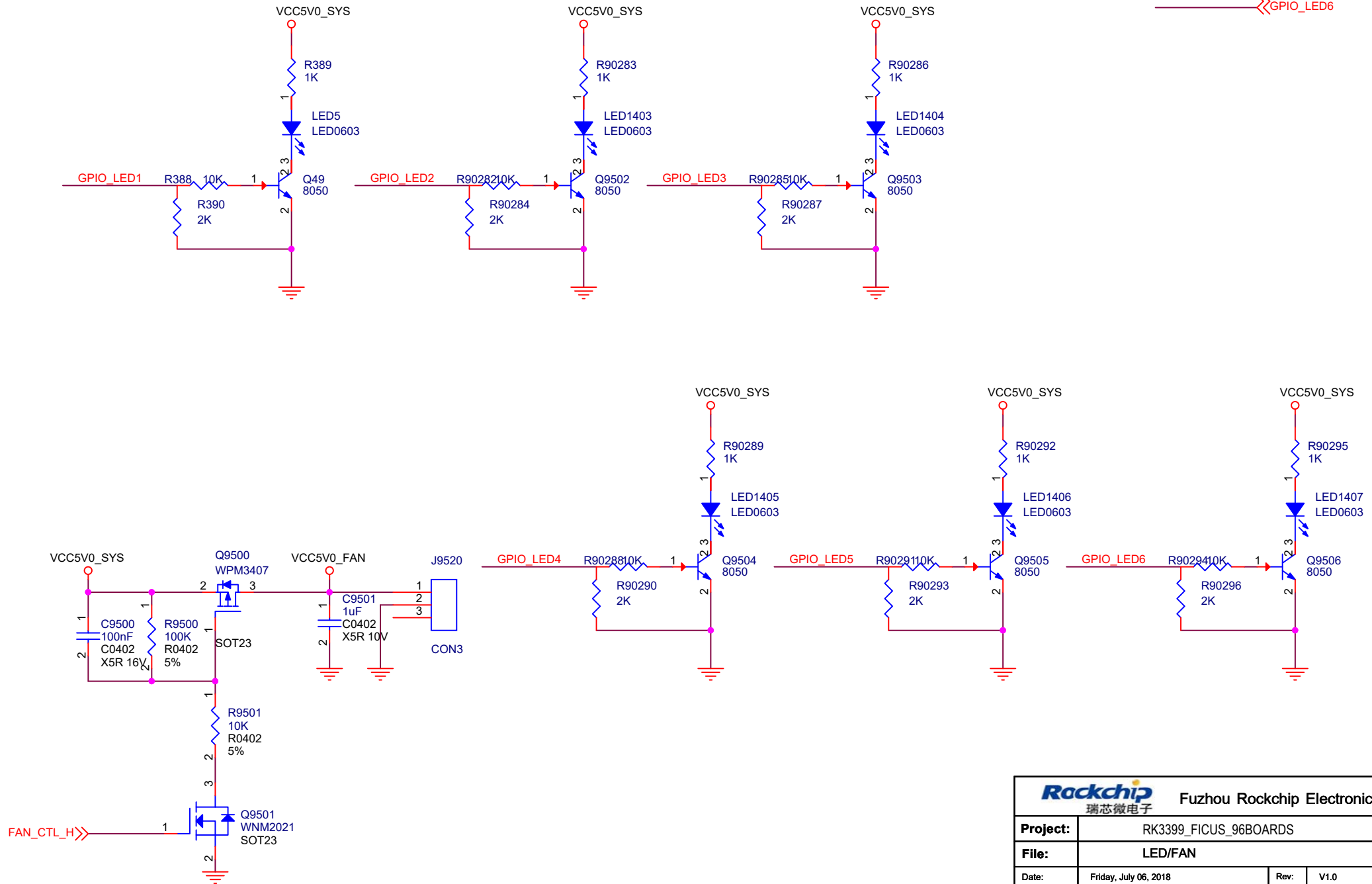



 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子			
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	IR&TP		
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# HEATSINK/FAN (option)

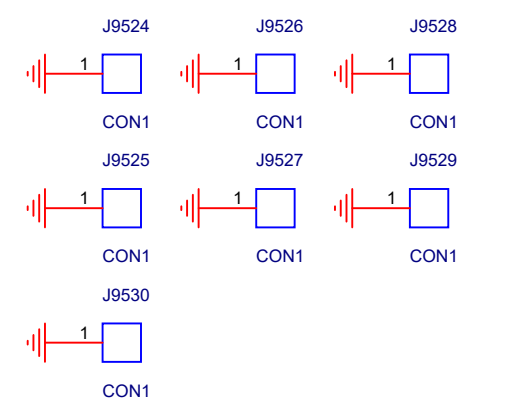
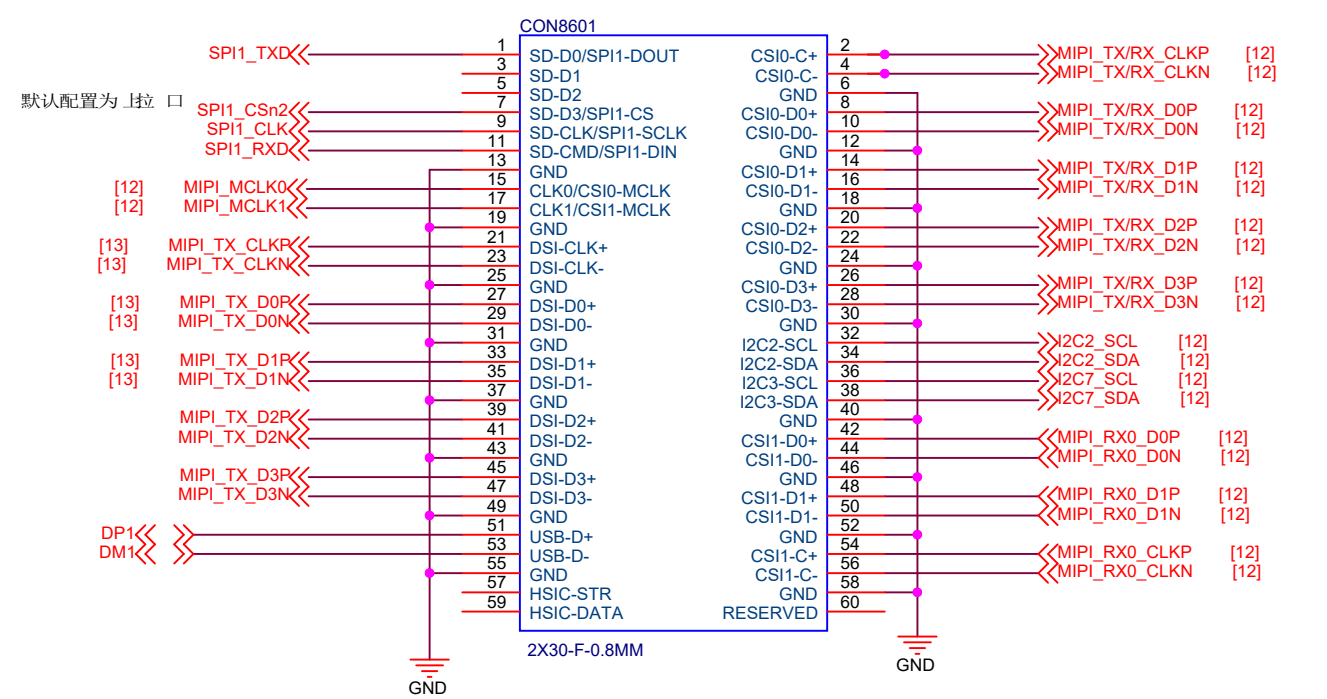
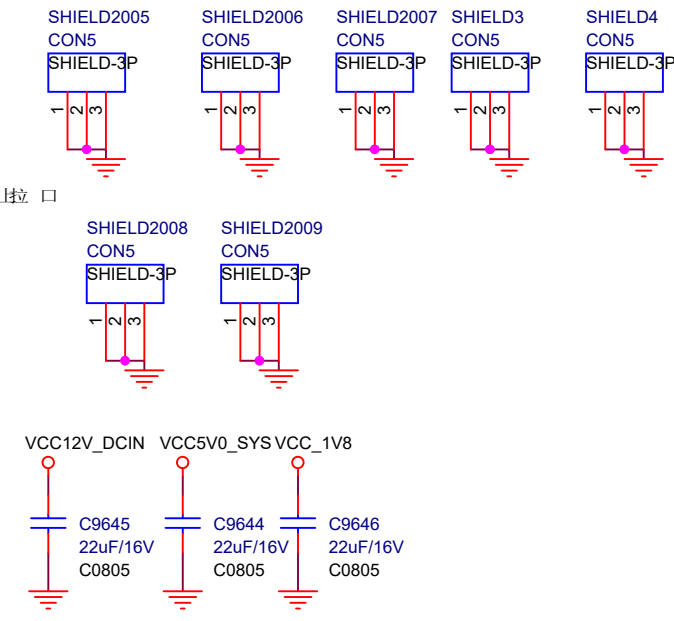
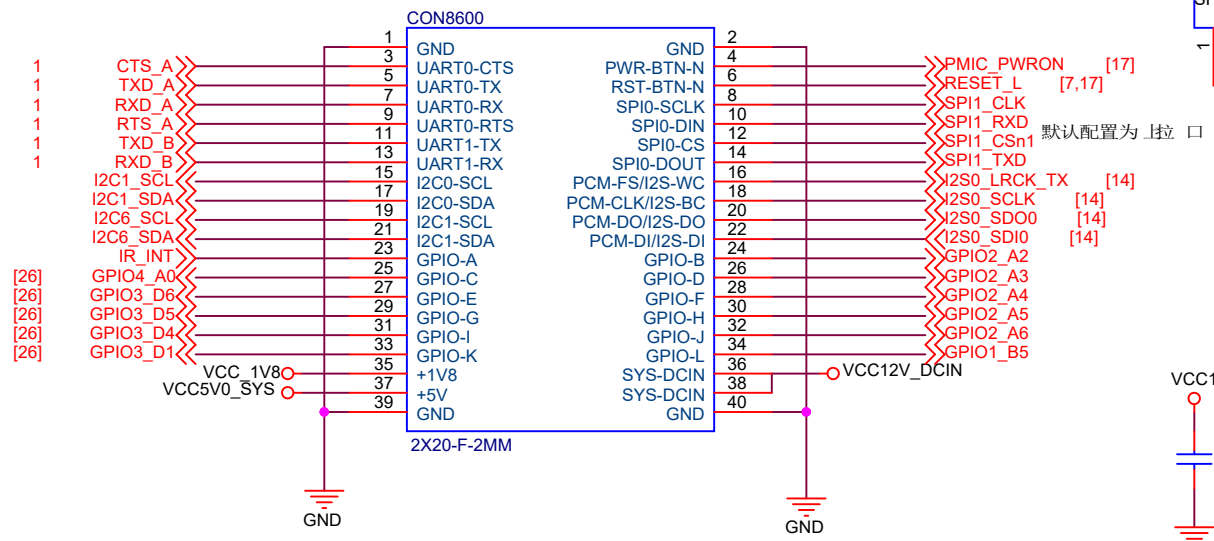
Note: Power for FAN, It can be delete if no need.

- GPIO\_LED1
- GPIO\_LED2
- GPIO\_LED3
- GPIO\_LED4
- GPIO\_LED5
- GPIO\_LED6



 <b>Fuzhou Rockchip Electronics</b> 瑞芯微电子	
<b>Project:</b>	RK3399_FICUS_96BOARDS
<b>File:</b>	LED/FAN
<b>Date:</b>	Friday, July 06, 2018
<b>Designed by:</b>	Linus
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<b>Rockchip</b> 瑞芯微电子		<b>Fuzhou Rockchip Electronics</b>	
<b>Project:</b>	RK3399_FICUS_96BOARDS		
<b>File:</b>	CONNECT		
<b>Date:</b>	Friday, July 06, 2018	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Linus	<b>Sheet:</b>	33 of 33